Sierra GPS Chipset
Leverage Trimble's wealth of GPS knowledge

Chips, support, and software from the GPS solutions company

Trimble's advanced Sierra™ (formerly Scorpion/Scott) chipset is now available to high-volume OEM customers for use in embedded applications. The Sierra™ chipset features state-of-the-art performance, small size, low power consumption, and low cost. The Sierra™ chipset consists of two ASICs, as well as fully developed software and unmatched technical support. The two ASICs are composed of Trimble's GPS DSP ASIC and an RF/IF down-converter chip.

Like a 32-valve V-8 engine, the 8-channel 32-correlator GPS DSP ASIC (Scorpion) is the powerful heart of Trimble's new line of Lassen™ and Palisade™ OEM receivers. The DSP ASIC has a 32-bit CPU and provides processing capability that guarantees industry-leading throughput and time-to-first-fix statistics. In addition, the on-chip serial ports and real-time clock reduce cost and simplify the task of integrating a GPS receiver into a host system. This ASIC can be operated at either 5V or, for significant power savings, 3.3V.

Inside the RF/IF ASIC (Scott), the 1575.42 MHz GPS signal is amplified and then downconverted through 2 stages to a pair of IF quadrature signals for processing by the DSP IC. This dual-down conversion scheme helps reduce power consumption without signal quality degradation. The final IF frequency is typically less than 1 MHz. This ASIC can be used in a design with the usual active antenna or passive antenna.

When you select the Sierra™ chipset, you are adding Trimble's GPS experience to your design. Trimble provides training that reduces design cycle time. Users can leverage Trimble's high volume manufacturing experience with a proven reference design that helps integrate GPS into the product smoothly. The Sierra™ chipset also includes a set of finished GPS firmware that needs no further software development. All these elements, as well as detailed schematics, a bill-of-materials, supplier lists, and manufacturing test programs create a package that ensures the shortest possible design times.
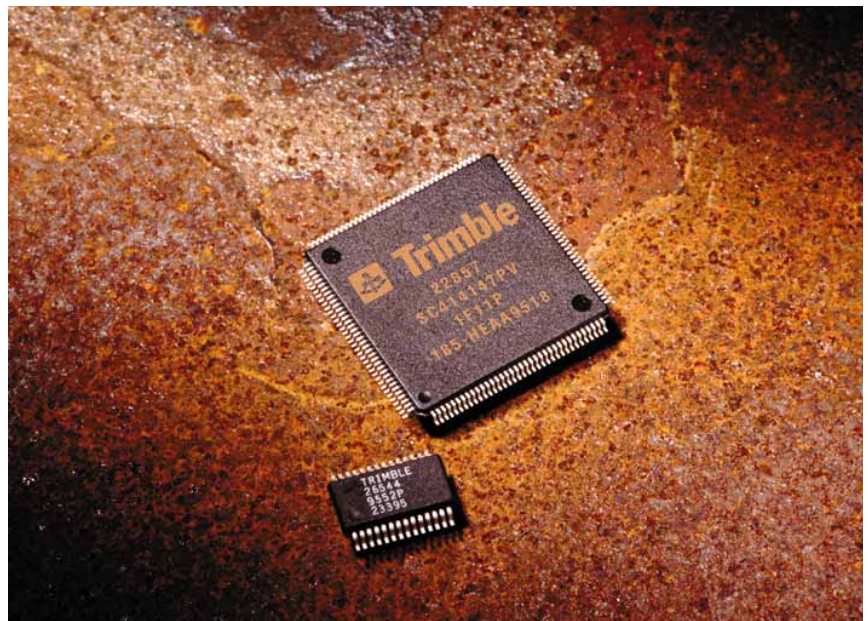
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Performance Specifications

General:	L1 frequency, C/A code (SPS), 8-channel continuous tracking receiver, 32 correlators.
Update rate:	TSIP @ 1 Hz: NMEA @ 1 Hz
Accuracy*:	Position: 25 m CEP (50%) without SA Velocity: 0.1 m/sec without SA Time: 500 nano-seconds (nominal)
DGPS accuracy:	Position: 2 m CEP (50%) Velocity: 0.05 m/sec Time: 500 nano-seconds (nominal)
Acquisition (typical):	Almanac aided start: <45 seconds (90%) Ephemeris aided start: <20 seconds (90%)
Reacquisition after signal loss	<2 seconds (90%)
Dynamics:	Altitude: +18,000 m maximum Velocity: 515 m/sec maximum Acceleration: 4g (39.2 m/sec^2) Motional Jerk: 20 m/sec^3

GPS ASIC

Description:	CMOS custom IC, containing 8 independent GPS channels, 32 correlators and embedded 68330 processor in a single chip.
Supply voltage:	5 volts DC ±5% or 3.3 volts DC ±10%
Board power consumption:	Varies depending on usage Typical total receiver power 5v: 700 mw 3.3v: 350 mw
Package:	144 TQFP (tested die also available)
Operating temp:	-40˚C to 85˚C

Ordering Information

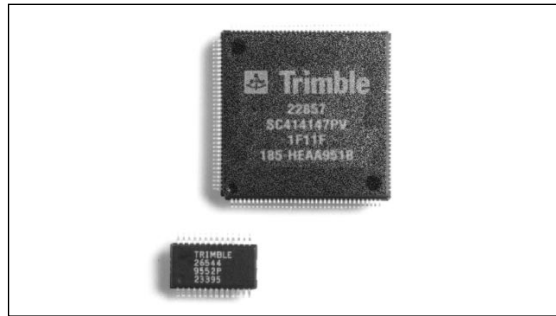29749-00   Sierra™ GPS Chipset includes the GPS ASIC and RF/IF ASIC.

* Note: All GPS receivers are subject to degradation of position and velocity accuracies under Department of Defense imposed Selective Availability (S/A).
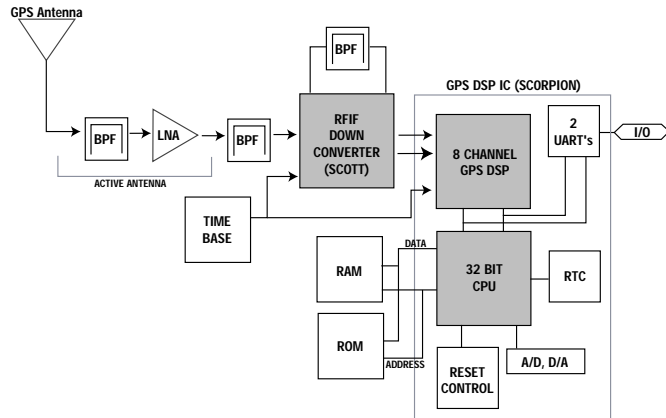
Specifications subject to change without notice.

www.trimble.com

RF/IF ASIC

Description:	GPS front end custom silicon bipolar IC containing dual down-converters and a frequency synthesizer.
Supply voltage:	5 volts DC ±5% or 3.3 volts DC ±10%
Power consumption:	5v: 160mw 3.3v: 100 mw
Package:	28 pin SSOP package (209 mil wide body)
Operating temp:	-40˚C to 85˚C

Actual size

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THE GPS SOLUTION