PRELIMINARY

MOSTEK®

3870 SINGLE CHIP MICRO FAMILY

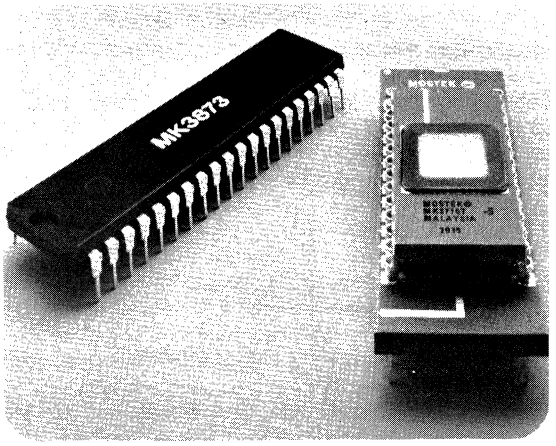
MK3873 and MK38P73

MK3873 FEATURES

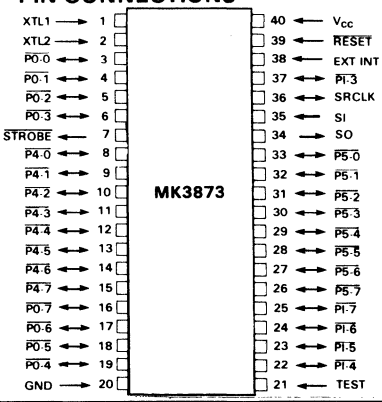
- ☐ Available with 1K or 2K byte mask programmable ROM
- ☐ Software compatible with 3870 instruction set
- ☐ 64 byte scratchpad RAM
- ☐ Available with 64 byte Executable RAM
- ☐ 29 bits (4 ports) TTL compatible parallel I/O
- ☐ Serial Input/Output port
  - External or Internal Serial Port Clock
  - Transmit and Receive registers double buffered
  - Internal Baud rate generator
  - Synchronous or Asynchronous serial I/O
  - Data rates to 9600 bits per second (ASYNC)
  - I/O pins dedicated as SERIAL IN, SERIAL OUT, and SERIAL CLOCK
  - Variable duty cycle waveform generation
- ☐ Vectored interrupts
- ☐ Programmable binary timer
  - Internal timer mode
  - Pulse width measurement mode
  - Event counter mode
- ☐ External Interrupt
- ☐ Crystal, LC, RC or external time base options available
- ☐ Low power (325 mW typ.)
- ☐ Single +5V power supply
- ☐ Pinout compatible with the 3870 Family members

MK38P73 FEATURES

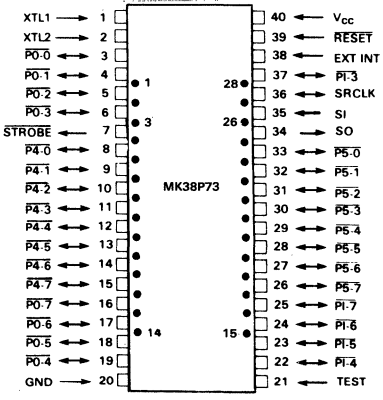
- ☐ EPROM version of MK3873
- ☐ Piggyback PROM (P-PROM)™ package
- ☐ Accepts 24 pin or 28 pin EPROM memories
- ☐ Identical pinout as MK3873
- ☐ In-Socket emulation of MK3873



MK3873 PIN CONNECTIONS



MK38P73 PIN CONNECTIONS



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GENERAL DESCRIPTION

The MK3873 single chip microcomputer introduces a major addition to the 3870 microcomputer family, a serial input/output port. This serial port is capable of either synchronous or asynchronous serial data transfers. The heart of the serial port is a 16-bit Shift Register that is double-buffered on transmit and receive. The Shift Register clock source can be either the internal baud rate generator or an external clock. An end-of-word vectored interrupt is generated in either transmit or receive mode so that the CPU overhead is only at the word rate and not at the serial bit rate. This serial channel can be used to provide a low-cost data channel for communicating between 3873 microcomputers or between a 3873 and another host computer. The serial port is also very flexible so that it could be used for other purposes such as an interface to external serial logic or serial memory devices.

The MK3873 retains commonality with the 3870 family of single chip microcomputers. It has up to 2048 bytes of mask ROM for program storage, and 64 bytes of scratchpad random-access memory. Certain versions also include up to 64 bytes of Executable RAM. Also, the 3870's sophisticated programmable binary timer is included and provides for system flexibility by operating in 3 different modes. The MK3873 has a large number of parallel I/O lines available to the user. Twenty nine pins of the MK3873 are dedicated to parallel I/O. In addition, three pins are dedicated to the serial I/O port. These pins provide input, output, and clock for the serial port. The serial clock pin can be driven externally or programmed to provide a 50% duty cycle TTL compatible serial clock. No additional CPU instructions are necessary for use with the serial port. Thus, the MK3873 is instruction set compatible with the rest of the 3870 family.

The MK38P73 microcomputer is the PROM based version of the MK3873 single-chip microcomputer. The MK38P73 is called the Piggyback PROM (P-PROM)™ microcomputer because of a new packaging concept. This concept allows a 24 or 28 pin EPROM to be mounted directly on top of the microcomputer itself. The EPROM can then be removed and reprogrammed as required with a standard PROM programmer. The MK38P73 retains exactly the same pinout and architectural features as other members of the MK3873 Family. The MK38P73 is discussed in more detail in a later section of this document.

FUNCTIONAL PIN DESCRIPTION

$\overline{P0\text{-}0}$ - $\overline{P07}$, $\overline{P1\text{-}3}$ - $\overline{P1\text{-}7}$, $\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$, $\overline{P5\text{-}0}$ - $\overline{P5\text{-}7}$ are 29 bidirectional I/O lines which can either be used as TTL compatible inputs or latch outputs.

SI - SERIAL IN is a TTL compatible Schmitt Trigger input pin for either serial synchronous or asynchronous data.

SO - SERIAL OUT is an output line for either serial synchronous or asynchronous data.

SRCLK is the clock for the serial port operations. It can be configured by software to be an input or output depending upon whether an internal baud rate or external clock is desired. It has a Schmitt trigger input and can be used to drive up to 3 TTL loads.

$\overline{STROBE}$ is a ready strobe associated with I/O Port 4. This pin which is normally high provides a single low pulse after valid data is present on the $\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$ pins during an output instruction. $\overline{STROBE}$ can be used to drive up to 3 TTL loads.

$\overline{RESET}$ may be used to externally reset the MK3873. When pulled low the MK3873 will reset. When allowed to go high the MK3873 will begin program execution at program location H'000'.

PIN NAME	DESCRIPTION	TYPE
$\overline{P0\text{-}0}$, $\overline{P0\text{-}7}$	I/O Port 0	Bidirectional
$\overline{P1\text{-}3}$ - $\overline{P1\text{-}7}$	I/O Port 1	Bidirectional
$\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$	I/O Port 4	Bidirectional
$\overline{P5\text{-}0}$ - $\overline{P5\text{-}7}$	I/O Port 5	Bidirectional
$\overline{STROBE}$	Ready Strobe	Output
EXT INT	External Interrupt	Input
$\overline{RESET}$	External Reset	Input
SI	Serial Input	Input
SO	Serial Output	Output
SRCLK	Serial Clock	Bidirectional
TEST	Test Line	Input
XTL 1, XTL 2	Time Base	Input
V_{CC}, GND	Power Supply Lines	Input

EXT INT is the external interrupt input. Its active state is software programmable as described in the 3870 Family Technical Manual. This input is also used in conjunction with the timer for pulse width measurement and event counting.

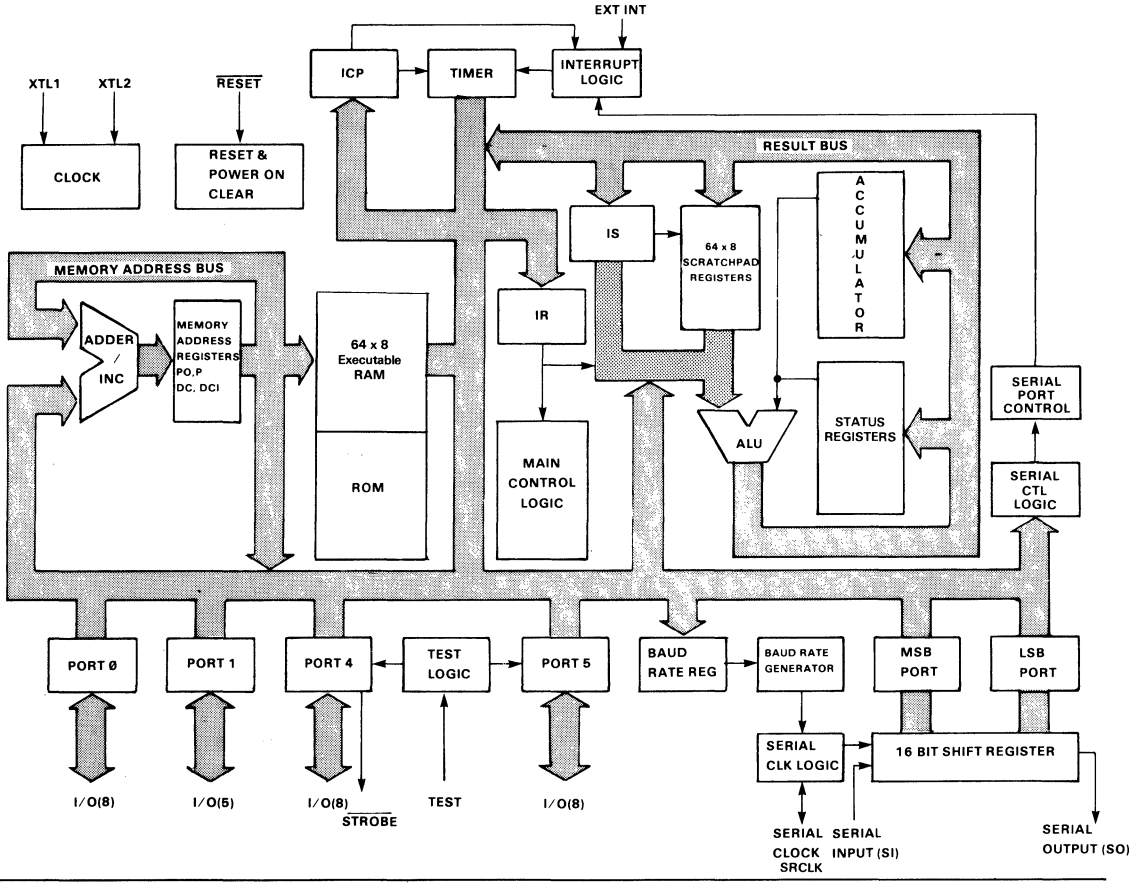
XTL 1 and XTL 2 are the time base inputs (2 MHz to 4 MHz) to which a crystal, LC network, RC network, or an external single-phase clock may be connected. The time base mode must be specified when submitting an order for a mask ROM MK3873. The MK38P73 will operate with any of the four configurations.

MK3873 ARCHITECTURE

The architecture of the MK3873 is identical to that of the rest of the devices in the 3870 family, with the exception of the serial port logic. The serial port logic is shown in the block diagram of the MK3873 (Figure 1). Addressing of the serial port logic is accomplished through I/O instructions. Operation and programming of the serial port is thoroughly discusssed below. A programming-model of the MK3873 is shown in Figure 2. For a more complete discussion of the 3870 family architecture, the user is referred to the 3870 Family Technical Manual.

MK3873 BLOCK DIAGRAM

Figure 1



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MAIN MEMORY

The main memory section on the MK3873 consists of a combination of ROM and executable RAM.

There are four registers associated with the main memory section. These are the Program Counter (PO), the Stack Register (P), the Data Counter (DC), and the Auxiliary Data Counter (DC1). The Program Counter is used to address instructions during program execution. P is used to save the contents of PO during an interrupt or subroutine call. Thus, P contains the return address at which processing is to resume upon completion of the subroutine or the interrupt routine. The Data Counter (DC) is used to address data tables. This register is auto-incrementing. Of the two data counters, only DC can access memory directly. However, the XDC instruction allows DC and DC1 to be exchanged.

The length of the PO, P, DC, and DC1 registers for all MK3873 devices is listed in the table shown in Figure 3. The graph and table in Figure 3 also shows the amounts of ROM and executable RAM for the different members of the MK3873 family.

EXECUTABLE RAM

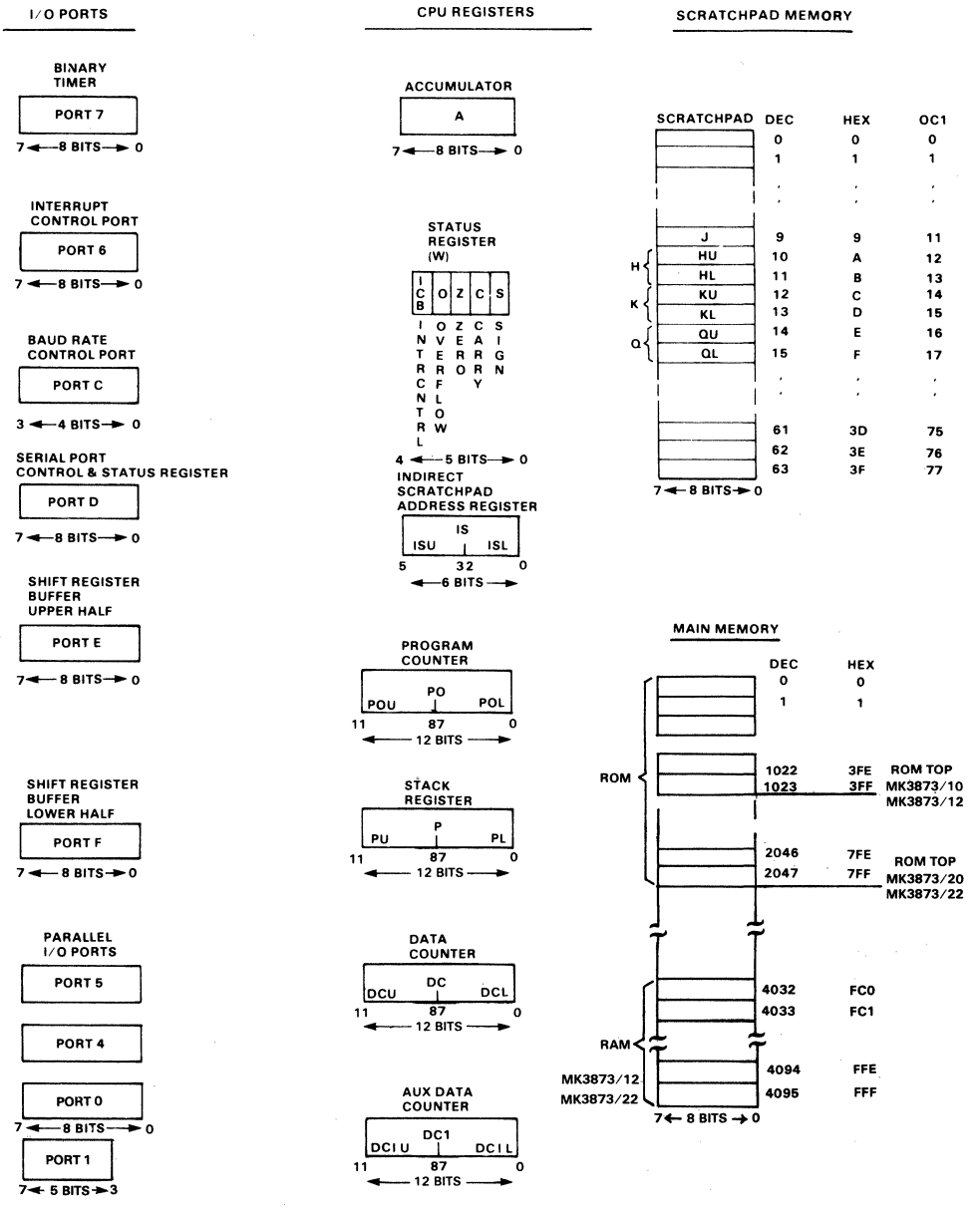
The upper bytes of the total address space in certain MK3873 devices is RAM memory. As with the ROM memory the RAM may be addressed by the PO and DC address registers. The executable RAM may be accessed by all 3870 instructions which address main memory indirectly through the Data Counter (DC) register. Additionally, the MK3873 may execute an instruction sequence which resides in the Executable RAM. Note that this cannot be done with the scratchpad RAM memory, which is the reason the term "Executable RAM" is given to this additional memory.

I/O PORTS

On the MK3873, 29 lines are provided for bidirectional, parallel I/O. These lines are addressable as four parallel I/O ports at locations 0, 1, 4, and 5. Note that Ports 0, 4, and 5 are 8 bits wide, while Port 1 contains only 5 bits of I/O in bit positions 3, 4, 5, 6, and 7. Bits 0-2 on Port 1 are not available for use as I/O port pins or as storage elements. The remaining three pins are used to provide the serial I/O

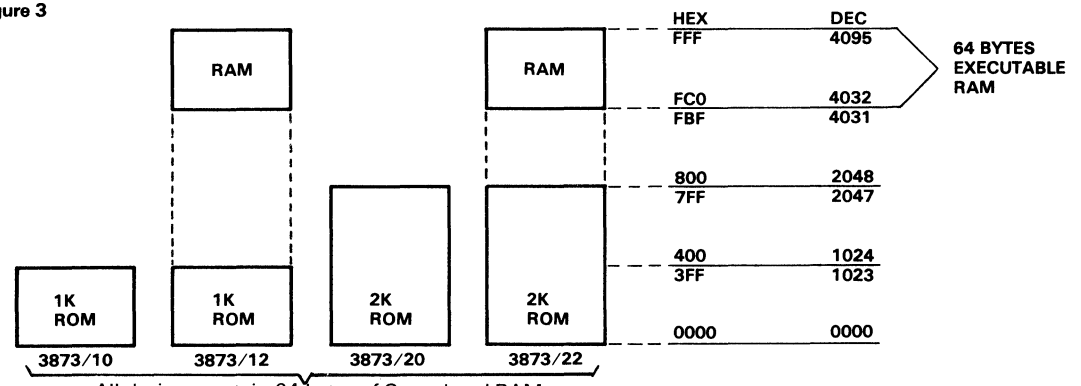
MK3873 PROGRAMMABLE REGISTERS, PORTS, AND MEMORY MAP

Figure 2



MK3873 MAIN MEMORY SIZES AND TYPES

Figure 3



All devices contain 64 bytes of Scratchpad RAM

Data derived from addressing any locations other than within the specified ROM and RAM space is not tested nor is it guaranteed. Users should refrain from entering this area of the memory map.

Device	Scratchpad RAM Size (Decimal)	Address Register Size P0, P, DC, DC1	ROM Size (Decimal)	Executable RAM Size
MK3873/10	64 bytes	12 bits	1024 bytes	0 bytes
MK3873/12*	64 bytes	12 bits	1024 bytes	64 bytes
MK3873/20	64 bytes	12 bits	2048 bytes	0 bytes
MK3873/22*	64 bytes	12 bits	2048 bytes	64 bytes

*The 3873/12 and 3873/22 will be available as future products.

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function. A conceptual schematic of a bidirectional I/O port pin and available output drive options are shown in Figure 4.

As in all other 3870 family devices, an output ready strobe is associated with Port 4. This flag may be used to signal a peripheral device that the 3873 has just completed an output of new data to port 4. The strobe provides a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. STROBE may also be used as an input strobe by doing a dummy output of H '00' to port 4 after completing the input operation.

SERIAL I/O OPERATION

The Serial Input/Output Port consists of a serial Shift Register, baud rate generator and control logic as shown in Figure 1. Together these elements provide the MK3873 with a half duplex asynchronous, or a full duplex synchronous, variable bit length serial port. Data is shifted into or out of the shift register at a rate determined by the internal baud rate generator or external clock. An end-of-word interrupt is generated in transmit or receive mode so that the CPU overhead is only at the word rate and not the serial bit rate.

SHIFT CLOCK

The internal clock is used to clock data transfers into and out of the 16 bit Shift Register. It is also used as an input to an internal counter which keeps track of the number of bits which have been shifted into or out of the Shift Register. Input data is sampled on the SERIAL INPUT, (SI), line on the rising edge of the SHIFT clock and is clocked into the most significant bit of the shift register. Output data is gated to the SERIAL OUTPUT line on the falling edge of the internal SHIFT clock.

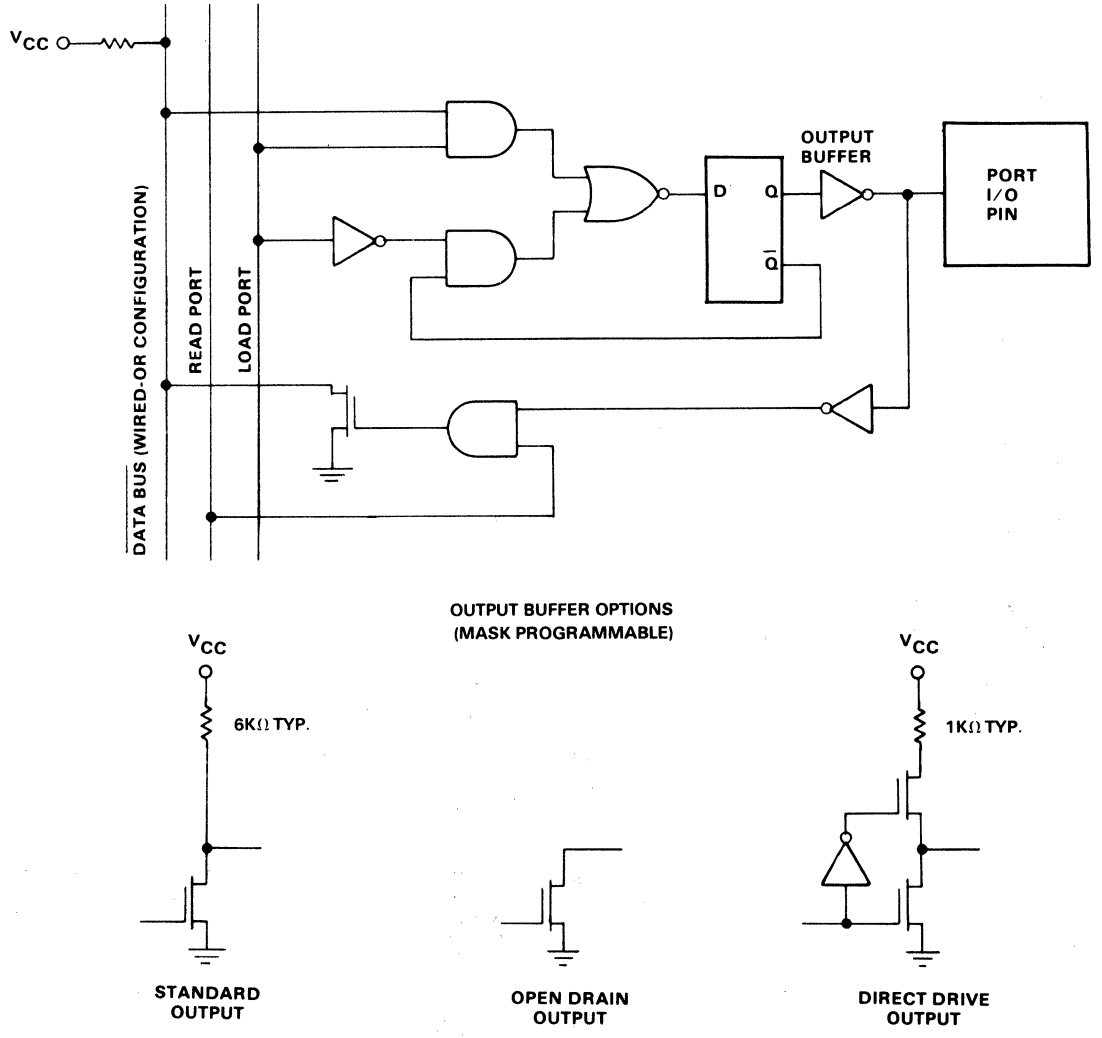
The clock is derived from the SRCLK pulse. The SRCLK pulse may be generated from the internal baud rate generator, or it may be programmed as an input. The internal SHIFT clock operates at the same frequency as the SRCLK pulse when the Sync mode is selected, and at a rate which is divided by 16 (÷16) from the SRCLK pulse when the Async mode is selected.

SHIFT REGISTER

The Serial Port Shift Register is a 16-bit serial to parallel, parallel to serial shift register. This register is addressed and double-buffered by ports E and F as shown in Figure 5A.

I/O PIN CONCEPTUAL DIAGRAM WITH OUTPUT BUFFER OPTIONS

Figure 4



Ports 0 and 1 are Standard Output type only.

Ports 4 and 5 may both be any of the three output options (mask programmable bit by bit)

The $\overline{\text{STROBE}}$ output is always configured similar to a Direct Drive Output except that it is capable of driving 3 TTL loads.

$\overline{\text{RESET}}$ and EXT INT may have standard 6KΩ (typical) pull-up or may have no pull-up (mask programmable). These two inputs have Schmitt trigger inputs with a minimum of 0.2 volts of hysteresis.

Serial In is a Schmitt trigger input with a minimum of 0.2V hysterisis.

Serial Out (SO) is the Standard Output type.

SRCLK output is capable of driving 3 TTL loads.

$\overline{\text{RESET}}$ and EXT INT do not have internal pull up on the MK38P73.

PORT D SERIAL PORT CONTROL REGISTER

The Serial Port Control register is write only and is addressed as Port D. The bit assignment is pictured in Figure 5C. The function of each bit is described below.

N2, N1, N0 - WORD LENGTH SELECT

These bits select one of the eight possible word lengths which are available with the MK3873 serial port. The serial port will shift the programmed number of bits through the Shift Register. If the Transmit mode is selected, data will be shifted out of the least significant bit (SR0) of the Shift Register to the Serial Out line (SO) while data is simultaneosly sampled at the Serial Input (SI) line and shifted into the most significant bit (SR15) of the Shift Register. When the Receive mode is selected, data will be sampled at SI and shifted in, but the SO line will be disabled such that it remains in a marking condition (Logic "1"). After the programmed number of bits have been shifted, the serial port logic will generate an end-of-word condition. This end-of-word condition will cause an interrupt if the serial port INTERRUPT ENABLE bit has been set.

It should be noted that the word values have been chosen so that the MK3873 can be programmed to send and receive a wide variety of asynchronous serial codes with various combinations of start and stop bits. Shown in Figure 6 is a table which gives the word length for various asynchronous data formats.

Values which would be programmed into the MK3873 Serial Port Register for Baudot, ASCII, and 8 bit binary codes in an asynchronous word format are shown in the table of Figure 6. Shown in the table are word length values for various combinations of data bits, start and stop bits, and parity. It can be seen that the MK3873 serial port can accommodate many different word lengths of asynchronous or synchronous data.

SERIAL PORT REGISTERS

Figure 5A

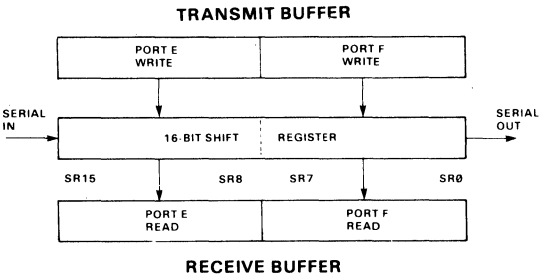


Figure 5B

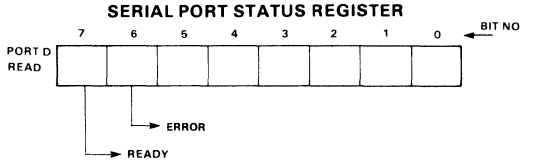
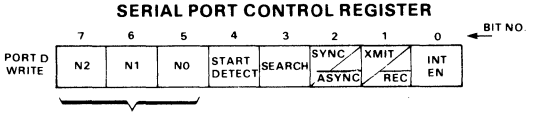


Figure 5C



WORD LENGTH SELECT

N2	N1	N0	WORD LENGTH
0	0	0	4 Bits
0	0	1	7 Bits
0	1	0	8 Bits
0	1	1	9 Bits
1	0	0	10 Bits
1	0	1	11 Bits
1	1	0	12 Bits
1	1	1	16 Bits

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ASYNCHRONOUS WORD LENGTHS

Figure 6

DATA WORD	# OF BITS	START BITS	STOP BITS	PARITY	WORD LENGTH (BITS)
BAUDOT	5	1	1	No	7
	5	1	2	No	8
	5	1	1	Yes	8
	5	1	2	Yes	9
ASCI I	7	1	1	No	9
	7	1	2	No	10
	7	1	1	Yes	10
	7	1	2	Yes	11
8 Bit Binary	8	1	1	No	10
	8	1	2	No	11
	8	1	1	Yes	11
	8	1	2	Yes	12

START DETECT

When the START DETECT bit is enabled the serial port will not shift data through the Shift Register until a valid start bit is detected at the SI input pin. The Start Detect mode is operative only when the Async mode has been selected by programming bit 2 of the Serial Port Control Register to a logic "0". By selecting the Async mode, the internal SHIFT clock frequency is divided by 16 from the clock frequency at the SRCLK pin. (Recall that SRCLK can be an input or an output depending on whether the internal baud rate generator or the external clock is selected). When the START DETECT bit is set, the serial port logic looks for a low level on the SI input on a SRCLK pulse edge. Until this low level occurs, the internal SHIFT clock is held low, and no data is shifted through the shift register. Once the level is sensed, the SI input will be sampled on every SRCLK pulse for seven clock periods. If the logic level remains at zero on the SI input for each of the seven clock periods, the serial port logic will begin shifting data into the Shift Register on the eighth SRCLK pulse. Data will be shifted in at the ÷16 or SHIFT clock rate until the number of bits have been shifted in. Once the programmed number of bits have been shifted, the start detect circuitry will be rearmed and will begin searching for the next high-to-low level on SI. This operation is pictured in the example shown in Figure 7.

When the START DETECT bit is disabled, data is continuously shifted through the Shift Register. An end-of-word condition will be generated each time the programmed number of bits has been shifted into or out of the Shift Register. A serial port interrupt will be generated when the end-of-word condition occurs, if it has been enabled.

SEARCH

The SEARCH bit is enabled by programming it to a logic "1". When enabled, the SEARCH bit causes the serial port logic to generate an interrupt at every bit time if the serial port interrupt has been enabled. This interrupt will occur regardless of whether or not the Transmit or Receive mode has been selected and whether or not the Synchronous or Asynchronous mode has been selected. The Search mode is usually used for recognition of a sync character in synchronous serial data transmission. The MK3873 serial port does not automatically detect sync characters.

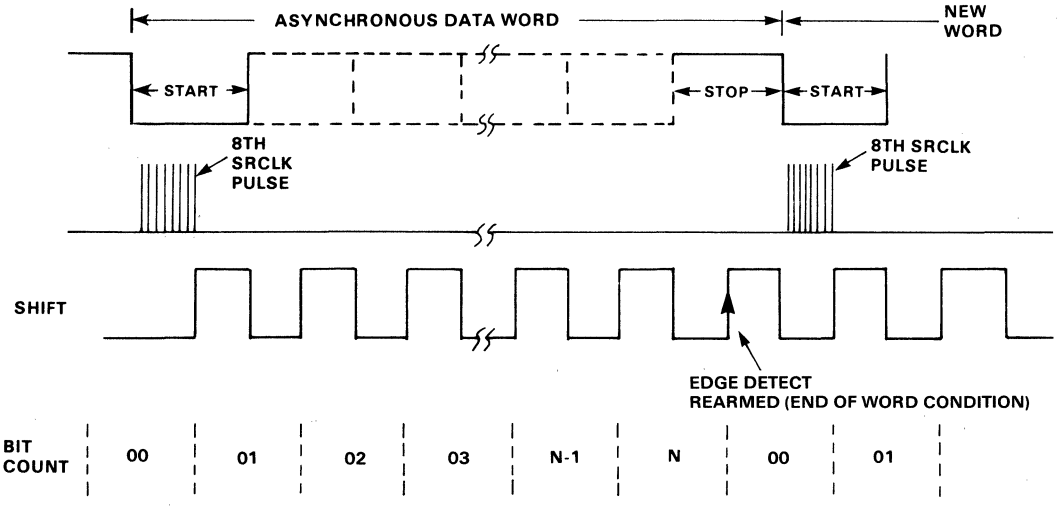
SYNC/ASYNC

The SYNC/$\overline{\text{ASYNC}}$ bit is used to select either the Synchronous mode of operation or the Asynchronous mode of operation. In the Synchronous mode of operation, data is shifted through the Shift Register at a rate which is ÷1 the rate of SRCLK. When the Synchronous mode is selected, the start bit detect circuitry cannot be enabled, even if the START DETECT bit is programmed to a "1". In the Asynchronous mode (SYNC/$\overline{\text{ASYNC}}$ = 0), the internal SHIFT clock operates at a rate which is ÷16 the rate of SRCLK.

XMIT/$\overline{\text{REC}}$

The XMIT/$\overline{\text{REC}}$ bit is used to select either the Transmit or Receive modes of operation. When programmed to a "1" XMIT is selected and the serial port will shift data on the SO line as well as shift data into the SI input. Transmitted data will be enabled on the SO output on the falling edge of the internal SHIFT clock. When the Receive mode is selected (by programming XMIT/$\overline{\text{REC}}$ = 0), data will be clocked into the Shift Register on the rising edge of SHIFT, as it is when the

MK3873 SERIAL PORT START BIT DETECTION
Figure 7



where N is the word length value selected by programming bits N2-N0 in the serial port control register

Transmit mode is enabled, but data will be disabled from being shifted out on Serial Out. Serial Out will be held at a marking, or logic "1", condition.

SERIAL PORT INTERRUPT ENABLE

By programming this bit to a "1", the serial port interrupt will be enabled. A serial port interrupt may then occur when an end-of-word condition is generated. Program control will be vectored to one of two locations upon a serial port interrupt, depending on the way the XMIT/$\overline{\text{REC}}$ bit has been programmed. If the Transmit mode has been selected by programming XMIT/$\overline{\text{REC}}$ bit to a "1", then program control will be vectored to location E0 (Hex). For the Receive mode (XMIT/$\overline{\text{REC}}$ = 0), program control will be vectored to 60 (Hex) when the serial port interrupt occurs. With the addition of the Serial Port Interrupt, the MK3873 has three sources of interrupt. If these three interrupts were to occur simultaneously, priority between them would be such that they would be serviced in the following order:

1) Serial Port
2) Timer
3) External Interrupt

STATUS REGISTER

Reading port D of the MK3873 by performing an Input or Input Short (IN or INS) instruction will load the contents of the Serial Port Status Register into the Accumulator. The two bits which make up the Status Register are shown in Figure 5B. The operation of these two bits is described below:

READY - The meaning of the READY flag depends on whether the Transmit or Receive mode is selected. When the Transmit mode has been selected, the READY flag is set when a Transmit Buffer empty condition occurs. This means that any previous data which may have been loaded into the Transmit Buffer register pair has been transferred into the Shift Register. Loading either byte of the Transmit Buffer will clear the READY flag until the time that the Transmit Buffer register pair is loaded into the Shift Register during an end-of-word condition

In the Receive mode (XMIT/$\overline{\text{REC}}$ = 0), the READY flag is used to indicate a Receive Buffer full condition. This means that a word of the programmed length has been shifted in and has been loaded into the receive buffer register pair. Reading one of the ports E or F which make up the receive buffer register pair will clear the READY flag. The READY flag will remain a 0 until the next word is completely shifted in and loaded into the receive buffer.

It should be noted that writing to the Serial Port Control Register has no effect on the state of the READY flag.

ERROR is like the READY flag; the meaning of ERROR depends on the programming of the XMIT/REC bit in the Serial Port Control Register. When the Transmit mode has been selected ERROR is used to indicate a transmitter underflow condition.

A transmitter underflow condition can occur as follows: Assume that the Transmit mode is selected. Suppose that a word is loaded into the Transmit Buffer register. The serial port logic will load the contents of the Transmit Buffer into the Shift Register and will begin to shift the word out on the SO pin. When the contents of the Transmit Buffer are loaded into the Shift Register, the serial port logic will signal the Transmit Buffer empty condition by setting the READY flag to a "1". When the word in the Shift Register is completely shifted out, an end-of-word condition will be generated. The serial port logic will then check to see if new data has been loaded into the Transmit Buffer. If it has not, the ERROR flag will be set, indicating that the serial port logic has run out of data to send. The ERROR flag can be used to signal an error condition to the firmware, or it can be used to signal that all data has been cleared out of the Shift Register for the purposes of line turnaround.

The ERROR flag which, in this case, represents a transmitter underflow condition, is reset by reading the Status Register.

When the Receive mode is programmed, ERROR is used to signal that the Receive Buffer has overflowed. This overflow condition can occur as follows: Suppose that a serial word is shifted in, generating an end-of-word condition. The serial port logic will load the contents of the Shift Register into the Receive Buffer, and will set the READY flag to a "1" to indicate that the Receive Buffer is full. When the next word being received is completely shifted in, generating the next end-of-word condition, the serial port logic will check to see if the Receive Buffer has been read by examining the state of the READY flag. If the READY flag = 0, then the previous word has already been read from the Receive Buffer by the software, and the serial port logic will load the current word into the Receive Buffer and will again set the READY flag. If the READY flag = 1, then the previous word has not been read from the Receive Buffer. The serial port logic will load the new word into the Receive Buffer, destroying the previous word. This action is signalled by the serial port logic setting the ERROR to a "1" signalling a receive buffer overflow condition. In this case, reading the status register also clears the ERROR flag.

BAUD RATE CONTROL REGISTER

Port C is designated as the Baud Rate Control register. Four bits, 0-3, are used to select nine different internal Baud rates or an external clock. When an internal Baud rate is programmed, the SRCLK output is generated at a frequency which is divided from the MK3873's time base frequency. The SRCLK frequency can be calculated by dividing the time base frequency by the divide factor shown in Figure 8 for the bit pattern which is programmed into bits C3-C0. Also shown in Figure 7 is the programming of bits C3-C0 to obtain a set of standard Baud rates when a 3.6864 MHz crystal is used as a time base.

BAUD RATE CONTROL PORT
PORT C WRITE ONLY
Figure 8

PORT C WRITE 7 6 5 4	3	2	1	0	Bit No.	SRCLK Divide Factor	Shift Clock Rate @ 3.6864 MHz time base SYNC	ASYNC
X X X X	C3	C2	C1	C0				
	1	0	1	1		÷24	153.6 kbs	9600 bps
	1	0	1	0		÷48	76.8 kbs	4800 bps
	1	0	0	1		÷96	38.4 kbs	2400 bps
	1	0	0	0		÷192	19.2 kbs	1200 bps
	0	1	1	1		÷384	9600 bps	600 bps
	0	1	1	0		÷768	4800 bps	300 bps
	0	1	0	1		÷1536	2400 bps	150 bps
	0	1	0	0		÷2096	1758.8 bps	110 bps
	0	0	1	1		÷3072	1200 bps	75 bps
	0	0	0	0		External Clock Mode		

When any of the internal Baud rates are selected, pin 36 becomes an output port pin. This pin is capable of driving three standard TTL inputs and provides a square wave output from the frequency selected in port C. The SYNC/$\overline{\text{ASYNC}}$ bit in the Serial I/O Control register has no effect on the output clock rate. The output will always be ÷1 directly from the Baud rate generator.

If all zeros are loaded into this port, the External Clock mode is selected. Pin 36 becomes an input. Any TTL compatible square wave input can be used to generate the clock for the serial port.

TRANSMIT AND RECEIVE BUFFERS

The Receive Buffer registers are two eight bit registers which are addressed as ports E and F (Hex) and are read only. The Receive Buffer registers may be read at any time. The Transmit Buffer registers are also two 8-bit registers which are write only and addressed as ports E and F (Hex).

In the Receive mode, the contents of the 16 bit Shift Register are transferred to the Receive Buffer Register pair when a complete word has been shifted in. Bits SR15-SR8 of the Shift Register are loaded into bits 7-0 of port E while bits SR7-SR0 are loaded into bits 7-0 of Port F.

When entering the Transmit mode, the first data transfer from the Transmit Buffer to the 16 bit Shift Register won't occur until a 1 word time delay after entering Transmit Mode.

In the Receive mode, no transfers between the Transmit Buffer and the 16 bit Shift Register can occur.

The serial port does not automatically right justify incoming data, nor does it insert or strip start and stop bits from an asynchronous data word. Therefore, it is usually necessary to right justify incoming data read from the Receive Buffer registers in software through shift instructions, as well as strip start and stop bits if an asynchronous data format is being used. Likewise, in transmitting an asynchronous data word, it is usually necessary to insert start and stop bits in software into the 16 bit word which is to be loaded in two halves into the Transmit Buffer register.

RESET

The reset circuit on the MK3873 is used to initialize the device to a known condition either during the course of program execution or on a power on condition. This section discusses the effect of $\overline{\text{RESET}}$ on the serial port logic. A more complete description of $\overline{\text{RESET}}$ may be found in the 3870 Family Technical Manual.

Upon reset, both the serial port control register (port D) and the Baud Rate Control register (port C) are loaded with zeroes. This action sets the serial port control logic in the following state:

N2, N1, N0 (word length) = 4 bits
START DETECT disabled
SEARCH disabled
Asynchronous Receive mode
Serial port interrupt disabled
External Clock mode (SRCLK = 1).
READY and ERROR are reset
Ports E and F are undefined

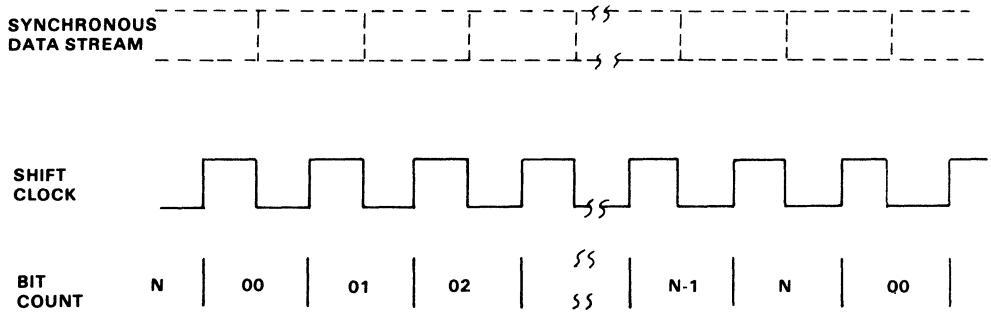
After the first control word is written to the Serial Port Control Register which selects an internal clock mode, the SRCLK will become an output and will remain high for one-half of a clock period as programmed into port C. It will then go low and produce a clock output waveform with the selected frequency.

ASYNCHRONOUS RECEIVE OPERATION

Figure 7 illustrates the timing for an example using the serial port in the Asynchronous mode. When operating in this mode, the Serial Port Control Register should be programmed for receive (XMIT/$\overline{\text{REC}}$ = 0) and the START DETECT bit should be enabled. Also, the Async mode should be selected, which allows the start detect circuitry to operate and sets the internal SHIFT clock at a rate which is divided by 16 (÷16) from the SRCLK rate. Upon selecting the Async mode and the START DETECT bit, the internal SHIFT clock is held low until a low level occurs on the SI pin. After a valid edge has been detected (see the START DETECT bit operation section), the SHIFT clock will go high and data will be shifted in at the middle of each bit time. When the programmed number of bits has been shifted in, an end-of-word condition is generated and a serial port receive interrupt will occur if it has been enabled.

After the falling edge of SHIFT following the end-of-word interrupt, the start detect circuitry will be enabled in preparation for the next word. Thus, if a start bit is present immediately following the time when the start detect circuitry is enabled, SHIFT Clock will again go high approximately on bit-time after the rising edge of SHIFT which clocked in the last bit of the preceding word and caused the end-of-word interrupt. In other words, SHIFT can go high again on

SYNCHRONOUS TRANSMIT OR RECEIVE TIMING
Figure 9



the eighth SRCLK pulse as soon as the start detect circuitry is rearmed.

The Shift Register must be read before the next end-of-word condition; otherwise, a receiver overrun error will occur. For a 9600 bps data rate, this would require reading the Receive Buffer within N x 104 μs from the time that the end-of-word condition is generated, where N is the number of bits in the data word.

The example in Figure 7 shows the timing required for asynchronous data reception from a device such as a teletype. Within this data stream are start, data and stop bits. A typical format requires 1 start bit, 8 data bits and 2 stop bits for a total of 11 bits. All of these bits will be residing in the 16 bit Shift Register when the end-of-word interrupt is generated. It is, therefore, necessary to strip the start and stop bits from the data.

SYNCHRONOUS RECEIVE OPERATION

For synchronous operation, the START DETECT bit should not be enabled and the XMIT/$\overline{\text{REC}}$ bit should be programmed to a zero. Also the Sync mode should be enabled so that the internal SHIFT clock is divided by 1, or is equivalent to, SRCLK. Once a control word is written to port D specifying START DETECT = 0, Receive mode, and Sync mode, then the Serial Port will continuously shift data into the MSB of the upper half of the Shift Register at the SRCLK rate and will generate an end-of-word condition when the programmed number of bits have been shifted in.

An illustration of synchronous receive timing is shown in Figure 9. This diagram is a synchronous receive sequence for a word which is N bits in length, where N corresponds to the number of bits which have been programmed into the Serial Port Control Register. Note the relationship of SHIFT clock, the synchronous data stream, and the bit count. Since the START DETECT bit is not enabled, the serial port logic will continuously shift data in and generate end-of-word conditions at regular intervals. When the end-of-word condition occurs, a serial port receive interrupt occurs if it has been enabled, and the contents of the Shift Register will be loaded into the Receive Buffer. The serial port logic will set the READY flag in the Serial Port Status Register, indicating that the receive buffer is full. Since the serial port is double-buffered on receive, the program has entire word time to read the Receive Buffer. At 9600 bps, this corresponds to a word time of N x 104μs, where N is the number of bits in a word.

Note that if a new control word is written to port D during the time that a serial word is shifted in, the bit count will be reset.

When using the Synchronous Receive mode on the MK3873, it is usually necessary to establish word synchronization in the data stream. The SEARCH bit, when enabled, causes the serial port logic to interrupt on each rising edge of SHIFT so that the data stream can be examined on a bit by bit basis. When the last bit of a sync word is found, the Search mode can be disabled and the serial port logic will shift in data and interrupt at the word rate.

ASYNCHRONOUS TRANSMIT OPERATION

The Asynchronous Transmit mode of operation is initiated by setting the XMIT/$\overline{\text{REC}}$ bit to a "1", and by programming the SYNC/$\overline{\text{ASYNC}}$ bit to a "0". Also, there must be an SRCLK pulse by selecting an internal or external source for SRCLK by programming port C. Upon setting XMIT/$\overline{\text{REC}}$ to a "1", there will be a 1 word length delay prior to the actual transfer of the first word from the Transmit Buffer to the 16 bit Shift Register. Serial data will then be shifted to the right on each rising edge of the internal SHIFT clock, and each new bit in the data stream will be enabled onto the SERIAL OUTPUT pin (SO) at the time of the falling edge of the

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internal SHIFT clock.

As mentioned, one word time delay is generated between the time that the Transmit mode is initiated by programming XMIT/$\overline{REC}$ = 1 and the time that the contents of the Transmit Buffer are transferred into the Shift Register. This word time delay is generated internally to the MK3873 by counting the number of SHIFT clock pulses which correspond to the number of bits programmed into the word length select section of the Serial Port Control Register (N2, N1, N0). Therefore, the word time delay is equivalent to the time it takes to shift a complete serial data word out of the Shift Register. The same word time delay will result if data had been loaded prior to programming the XMIT/$\overline{REC}$ bit to a "1". As mentioned in the "START DETECT" bit description, the internal SHIFT clock is disabled when this bit is programmed to a "1". Since the serial port logic counts SHIFT clock pulses to generate the word time delay, the Transmit Buffer contents will never be transferred to the Shift Register and shifted out when the START DETECT bit is enabled. Also, the Transmit Buffer contents cannot be loaded into the Shift Register when XMIT/$\overline{REC}$ bit = 0.

When the initial serial data word has been transferred into the Shift Register, the READY flag is set in the Serial Port Status Register, which is used to indicate that the Transmit Buffer is empty. A transmit interrupt will be generated if the INTERRUPT ENABLE bit has been set in the Serial Port Control Register, and program control will be vectored to location E0 (hex). When operating the serial port in a polled environment with the serial port interrupt disabled, the READY bit can be used as a flag which indicates that new data may be loaded into the Transmit Buffer. In an interrupt driven software configuration, new data may be loaded into the Transmit Buffer at the beginning of the serial port interrupt service routine.

During the operation of the Transmit Mode, the SERIAL INPUT pin (SI) is sampled and shifted into the Shift Register. However, since the START DETECT bit must be disabled during a transmit sequence, there is no way of establishing bit synchronization on any incoming serial data. Therefore, in the Asynchronous mode, the serial port can only be used in a half-duplex configuration.

After a block of data has been sent, it is sometimes useful for the program to know when the last serial word has been shifted out of the shift register. This is especially useful when operating the MK3873 with a bidirectional half-duplex transmission line. Once the block of serial data has been completely shifted out of the port, then it is usually desirable to reverse the direction of the line so that data may be received.

One way of determining when the last word has been shifted out of the Shift Register is through the use of the ERROR status bit in the Serial Port Status Register. The sequence would take place as follows: the program loads the Transmit Buffer with the last serial data word which is to be sent out either when the "READY" bit is set or during a transmit interrupt service routine. Loading the Transmit Buffer clears the READY flag. At the next end-of-word condition, the last serial data word is transferred from the Transmit Buffer into the Shift Register, which sets the READY flag once again. At this point the program will not load any more data into the Transmit Buffer and the READY flag will remain set. When the last word is completely shifted out of the Shift Register, the serial port logic will check to see if any new data has been loaded into the Transmit Buffer register pair. When it determines that there are no new data in the Transmit Buffer, the serial port logic will set the ERROR bit in the serial port status register and will return the SERIAL OUTPUT pin (SO) to a making condition (logic "1"). The SERIAL OUTPUT pin (SO) is always returned to a marking condition on transmitter underflow when the ASYNC mode is selected. Since the ERROR bit is set when the last serial data word has completely been sent out, it can be used as a signal to indicate the end of transmission and that the direction of the transmission line may be set for receive.

SYNCHRONOUS TRANSMIT OPERATION

The Synchronous Transmit mode of operation is selected by programming bit 2 (XMIT/$\overline{REC}$) of the Serial Port Control register to a "1" and setting the SYNC/$\overline{ASYNC}$ bit to a "1".

Figure 9 illustrates serial output timing relationships in the Synchronous mode. Data are shifted to the right on each rising edge of the internal SHIFT clock. Output data are not enabled to the SERIAL OUTPUT pin (SO) until the falling edge of the SHIFT clock. In a 16 bit data word, SR0, the least significant bit of the Shift Register is shifted out first, and SR15, the most significant bit of the Shift Register, is shifted out last. While the Shift Register contents are being output on a bit by bit basis, data are simultaneously shifted in to the Shift Register through the SI pin.

As discussed in the "ASYNCHRONOUS TRANSMIT OPERATION" section, a word time delay is generated between the time that data is written to the Transmit Buffer and the time that the contents of the Transmit Buffer are loaded into the Shift Register once the XMIT/$\overline{REC}$ bit has been programmed to a one (1).

Another way of loading the initial data word into the Transmit Buffer requires that the word synchronization be achieved through recognition of a received sync character. Recall that in the Transmit mode, data are sampled at SI and shifted into the Shift Register at the same time that data are shifted out through SO. Upon power up or reset, a control word may be written to Port D which specifies Transmit and Synchronous modes. Word synchronization can then be achieved through the use of the SEARCH bit as described in the section which covers Synchronous Receive mode. Once word synchronization is achieved, the SEARCH bit is disabled and the serial port shifts in data and generates an end-of-word condition at the word rate.

Each time the end of word condition is reached, receive data

is transferred from the shift register into the Receive Buffer. At the same time, data is transferred from the Transmit Buffer into the Shift Register.

Therefore, in the Synchronous Transmit mode, the serial port may be used in a full duplex mode if word synchronization is established. At each end of word condition, output data is transferred to the Shift Register from the Transmit Buffer. At the same time, an incoming data word is transferred from the Shift register to the Receive Buffer register pair. In this case, the End-of-Word transmit routine would be used for sending data by loading the Transmit Buffer register, and for receiving data by reading the Receive Buffer register. Note that once word synchronization is established, an amount of time which is equal to one word time is available following the end-of-word interrupt for loading data into the Transmit Buffer.

The serial port operates differently in the Transmit mode for Synchronous operation that it does for Asynchronous operation. In the Asynchronous mode, after a word has been shifted out, the SO line is returned to a marking condition if no new data have been loaded into the Transmit Buffer.

In the Synchronous mode, after a word has been shifted out, the contents of the Transmit Buffer are loaded into the Shift Register regardless of whether or not new data were loaded into the Transmit Buffer. If new data were not loaded since the last time the transmit buffer was read, the ERROR flag is set and signals a transmitter underflow condition. This feature of always reloading the Shift Register with the contents of the Transmit Buffer when an end-of-word condition occurs allows a sync word to be continuously generated without CPU intervention when the transmitter is idle. This feature also allows for a variable duty cycle, variable frequency waveforms to be generated on the Serial Output line.

MK38P73 GENERAL DESCRIPTION

The MK38P73 is the EPROM version of the MK3873. It retains an identical pinout with the MK3873. The MK38P73 is housed in the "R" package which incorporates a 28 pin socket located directly on top of the package.

The MK38P73 can act as an emulator for the purpose of verification of user code prior to the ordering of mask ROM MK3870 devices. Thus, the MK38P73 eliminates the need for emulator board products. In addition, several MK38P73s can be used in prototype systems in order to test design concepts in field service before committing to high-volume production with mask ROM MK3873s. The compact size of the MK38P73/EPROM combination allows the packaging of such prototype systems to be the same as that used in production.

Finally, in low-volume applications, the MK38P73 can be used as the actual production device.

Most of the material which has been presented for the MK3873 applies to the MK38P73. The MK38P73 has the same architecture and pinout as the MK3873. Additional information is presented in the following sections.

MK38P73 MAIN MEMORY

As can be seen from the block diagram in Figure 10, the MK38P73 contains no on-chip ROM. The memory address and data lines are brought out to the 28 pin socket located directly on top of the 40 pin package. The MK38P73 will address up to 4096 bytes of external EPROM memory.

There is one memory version of the MK38P73, and it is designated as the MK38P73/02. The MK38P73/02 contains 64 bytes of on-chip executable RAM. The MK38P73/02 can emulate the following mask ROM MK3873 devices:

MK3873/10
MK3873/12
MK3873/20
MK3873/22

Addressing of main memory on the MK38P73 is accomplished in the same way as it is for the MK3873. See Figure 12 for Main Memory addresses and for address register size in the MK38P73.

MK38P73 EPROM SOCKET

A 28 pin EPROM socket is located on top of the MK38P73 "R" package. The socket and compatible EPROM memories are shown in Figure 11. When 24 pin memories are used in the 28 pin socket, they should be inserted so that pin 1 of the memory device is plugged into pin 3 of the socket. (The memory should be lower justified in the 28 pin socket.)

The 28-pin socket has been provided to allow use of both 24-pin and 28-pin memory devices. Minor pin-out differences in the memory devices must be accommodated by providing different versions of the MK38P73.

Initially, the MK38P73 that is compatible with the MK2716 is available. The MK38P73 designed to accommodate the 28-pin memory devices will be available at a later date.

MK38P73 I/O PORTS

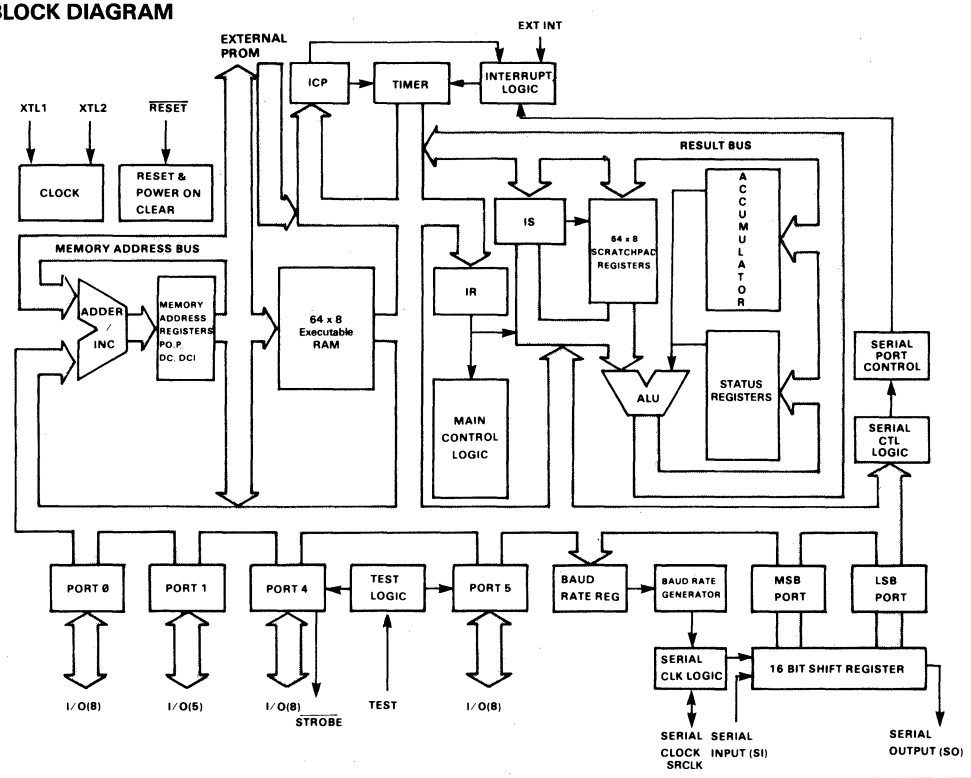
The MK38P73 is offered with open drain type output buffers on Ports 4 and 5. This open drain version is provided so that user-selected open drain port pins on the mask ROM MK38P73 can be emulated prior to ordering those mask ROM parts. Figure 11 lists the part ordering number for an MK38P73/02.

MEMORY ACCESS TIMING

A timing diagram depicting the memory access timing of the MK38P73 is shown in Figure 13. The Φ clock signal is

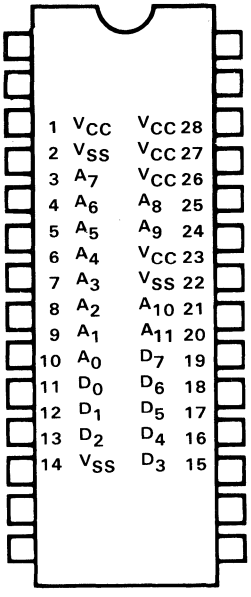
MK38P73 BLOCK DIAGRAM

Figure 10



MK38P73 "R" PACKAGE PINOUT

Figure 11



MK97310 (Open Drain)
Compatible Memories
2758
MK2716
2516 2532

derived internally in the MK38P73 by dividing the time base frequency by two and is used to establish all timing frequencies. The WRITE signal is another internal signal to the MK38P73 which corresponds to a machine cycle during which time a memory access may be performed. Each machine cycle is either 4 Φ clock periods or 6 Φ clock periods long. These machine cycles are termed short cycles and long cycles respectively. The worst case memory cycle is the short cycle, during which time an op code fetch is performed. This is the cycle which is pictured in the timing diagram. After a delay from the falling edge of the WRITE clock, the address lines A_{11} - A_0 become stable. Data must be valid at the data out lines of the PROM for a setup time prior to the next falling edge of the WRITE pulse. The total access time available for the MK38P73 is shown as t_{aas}, or the time from when address is stable to when data must be valid on the data bus lines.

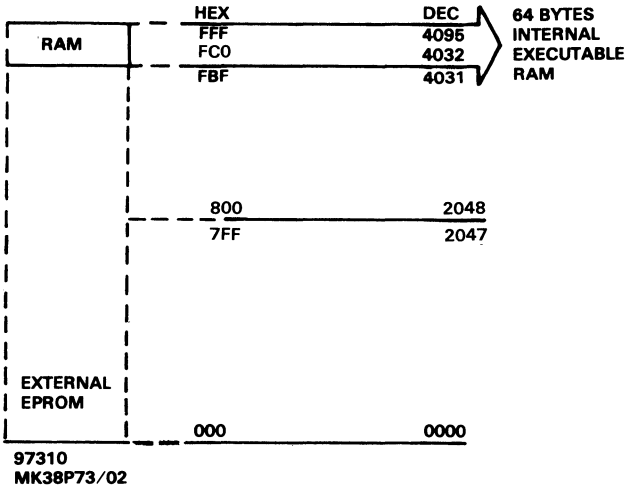
An equation for calculating available memory access time and some calculated access times based on the listed time base frequencies is also shown in Figure 13.

3873 TIME BASE OPTIONS

The 3873 contains an on-chip oscillator circuit which provides an internal clock. The frequency of the oscillator circuit is set from the external time base network. The time

MK38P73 MAIN MEMORY MAP

Figure 12



Device	Scratchpad RAM Size (Decimal)	Address Register Size P0, P, DC, DC1)	ROM Size (Decimal)	Executable RAM Size
MK38P73/02 97310	64 bytes	12 bits	0 bytes	64 bytes

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base for the 3873 may originate from one of four sources:

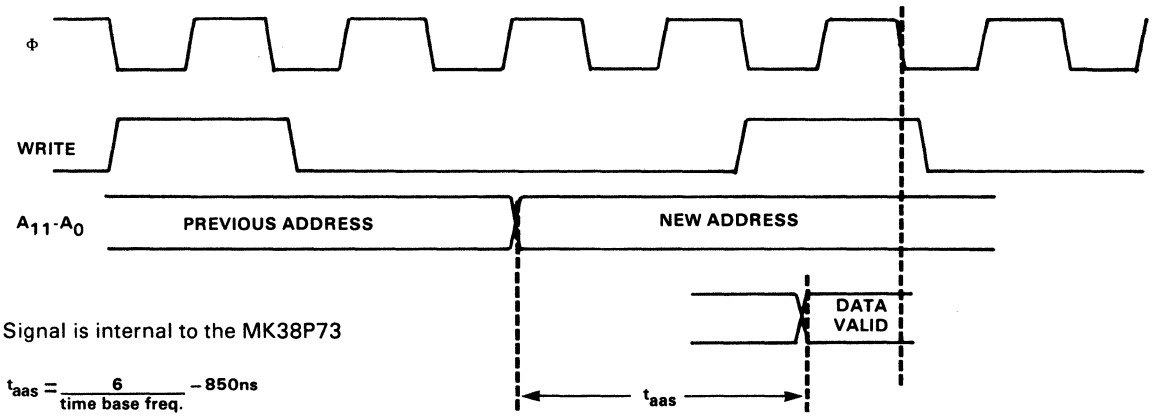
1) Crystal
2) LC Network
3) RC Network
4) External Clock

The type of network which is to be used with the mask ROM MK3873 must be specified at the time when mask ROM devices are ordered. However, the MK38P73 may operate with any of the four configurations so that it may emulate any configuration used with a mask ROM device.

The specifications for the four configurations are given in the following text. There is an internal 26pF capacitor between XTL 1 and GND and an internal 26pF capacitor between XTL 2 and GND. Thus, external capacitors are not necessarily required. In all external clock modes the external time base frequently is divided by two to form the internal PHI clock.

MEMORY ACCESS SHORT CYCLE OP CODE FETCH MK38P73

Figure 13



Signal is internal to the MK38P73

$$t_{aas} = \frac{6}{\text{time base freq.}} - 850ns$$

(FROM ADDRESS STABLE)

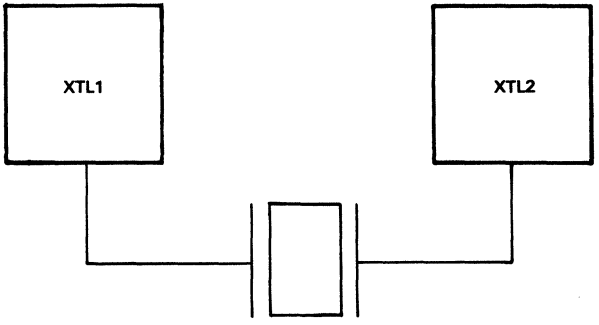
	4MHz	3.58MHz	3MHz	2.5MHz	2MHz
ACCESS TIME	650ns	825ns	1.15μs	1.55μs	2.15μs

CRYSTAL SELECTION

The use of a crystal as the time base is highly recommended as the frequency stability and reproductiveness from system to system is unsurpassed. The 3873 has an internal divide by two to allow the user of inexpensive and widely available TV Color Burst Crystals (3.58MHz). Figure 15 lists the required crystal parameters for use with the 3873. The Crystal Mode time base configuration is shown in Figure 14.

CRYSTAL MODE CONNECTION

Figure 14



CRYSTAL PARAMETERS
Figure 15

a) Parallel resonsnace, fundamental mode AT-Cut
b) Shunt capacitance (C_0) = 7 pf max.
c) Series resistance (R_S) = See table
d) Holder = See table below.

Frequency	Series Resistance	Holder
f = 2-2.7 MHz	Rs = 300 ohms max	HC-6 HC-33
f = 2.8-4 MHz	Rs = 150 ohms max	HC-6 HC-18* HC-25* HC-33

*This holder may not be available at frequencies near the lower end of this range.

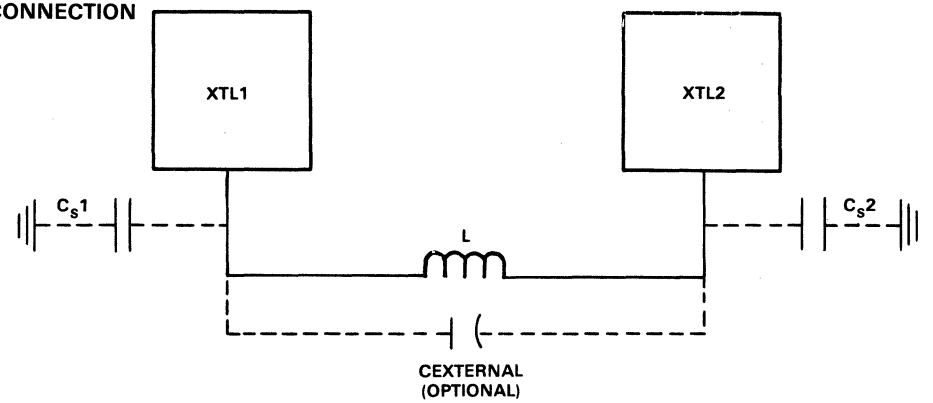
Through careful buffering of the XTL1 pin it may be possible to amplify this waveform and distribute it to other devices. However, Mostek recommends that a separate active device (such as a 7400 series TTL gate) be used to oscillate the crystal and that the waveform from that oscillator be buffered and supplied to all devices, including the 3873, in the event that a single crystal is to provide the time base for more than just a single 3873.

While a ceramic resonator may work with the 3873 crystal oscillator, it was designed specifically to support the use of this component. Thus, Mostek does not support the use of a ceramic resonator either through proper testing, parametric specification, or applications support.

LC NETWORK

The LC time base configuration can be used to provide a less expensive time base for the 3873 than can be provided with a crystal. However, the LC configuration is much less accurate than is the crystal configuration. The LC time base configuration is shown in Figure 16. Also shown in the figure are the specified parameters for the LC components, along with the formula for calculating the resulting time base frequency. The minimum value of the inductor which is required for proper operation of the LC time base network is 0.1 millihenries. The inductor must have a Q factor which is no less than 40. The value of C is derived from C external, the internal capacitance of the 3873, C_{XTL}, and the stray capacitances, C_{S1} and C_{S2}. C_{XTL} is the capacitance looking into the internal two port network at XTL1 and XTL2. C_{XTL} is listed under the "Capacitance" section of the Electrical Specifications. C_{S1} and C_{S2} are stray capacitances from XTL1 to ground and from XTL2 to ground, respectively. C external should also include the stray shunt capacitance across the inductor. This is typically in the 3 to 5 pf range, and significant error can result if it is not included in the frequency calculation.

LC MODE CONNECTION
Figure 16



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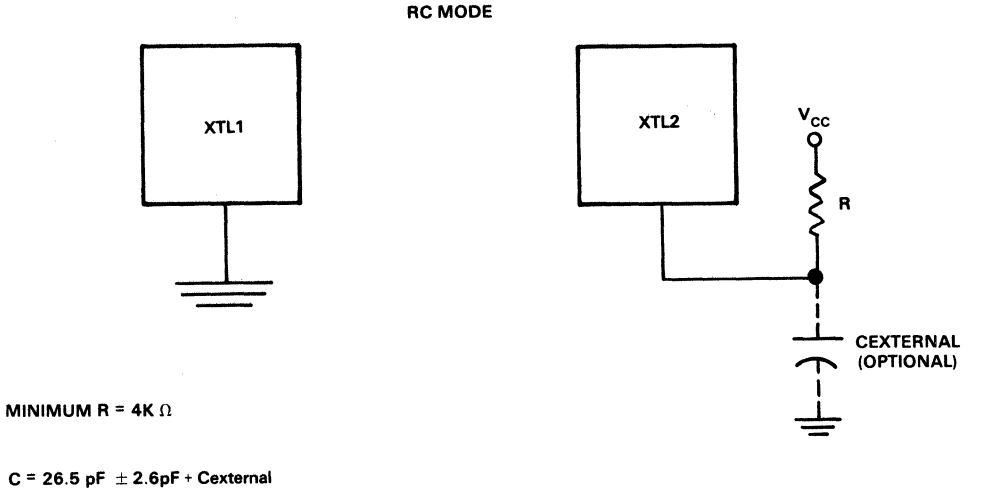
Variation in time base frequency with the LC network can arise from one of four sources: 1) Variation in the value of the inductor. 2) Variation in the value of the external capacitor. 3) Variation in the value of the internal capacitance of the 3873 at XTL1 and XTL2, and 4) Variation in the amount of stray capacitance which exists in the circuit. Therefore, the actual frequency which is generated by the LC circuit is within a range of possible frequencies, where the range of frequencies is determined by the worst case variation in circuit parameters. The designer must select component values such that the range of possible frequencies with the LC mode does not go outside of the specified operating frequency range for the 3873.

RC CLOCK CONFIGURATION

The time base for the 3873 may be provided from an RC network tied to the XTL2 pin, when XTL1 is grounded. A schematic picturing the RC clock configuration is shown in Figure 17. The RC time base configuration is intended to provide an inexpensive time base source for applications in which timing is not critical. Some users have elected to tune each unit using a variable resistor or external capacitor, thus reducing the variation in frequency. However, for increased time base accuracy, Mostek recommends the use of the Crystal or LC time base configuration. Figure 18 illustrates a curve which gives the resulting operating frequency for a particular RC value. The x-axis represents the product of the value of the resistor times the value of the capacitor. Note that three curves are actually shown. The curve in the middle represents the nominal frequency obtained for a given value of RC. A maximum curve and a minimum curve for different types of 3873 devices are also shown in the diagram.

RC MODE CONNECTION
Figure 17



The designer must select the RC product such that a frequency of less than 2 MHz is not possible, taking into account the maximum possible RC product and using the minimum curve shown in Figure 18. Also, the RC product must not allow a frequency of more than 4 MHz, taking into account the minimum possible R and C and using the Maximum curve shown. Temperature induced variations in the external components should be considered in calculating the RC product.

Frequency variation from unit to unit due to switching speed and level at constant temperature and V_{CC} = + or - 5 percent.

Frequency variation due to V_{CC} with all other parameters constant with respect to +5V = +7 percent to -4 percent on all devices.

Frequency variation due to temperature with respect to 25 C (all other parameters constant) is as follows:

PART #	VARIATION
387X-00, -05	+6 percent to - 9 percent
387X-10, -15	+9 percent to -12 percent

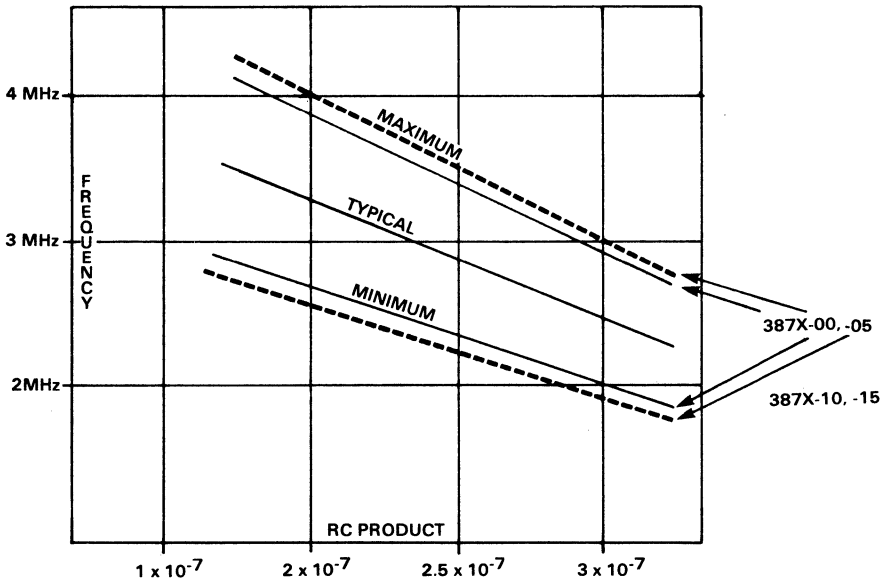
Variations in frequency due to variations in RC components may be calculated as follows:

Maximum RC = (R max) (C external max + C_{XTL} max)

Minimum RC = (R min) (C external min + C_{XTL} min)

$$\text{Typical RC} = (\text{R typ})\left(\text{C external typ} + \frac{\{C_{XTL}\ \text{max} + C_{XTL}\ \text{min}\}}{2}\right)$$

FREQUENCY VS. RC
Figure 18



Positive Freq. Variation = RC typical - RC minimum / RC typical

Negative Freq. Variation = RC maximum - RC typical / RC typical
due to RC Components

Total frequency variation due to all factors:

387X-00, -05
= +18 percent plus positive frequency variation due to RC components

= -18 percent minus negative frequency variation due to RC components

387X-10, -15
= +21 percent plus positive frequency variation due to RC components

= -21 percent minus negative frequency variation due to RC components

Total frequency variation due to V_{CC} and temperature of a unit tuned to frequency at +5V V_{CC}, 25 C

387X-00, -05
= + 13 percent

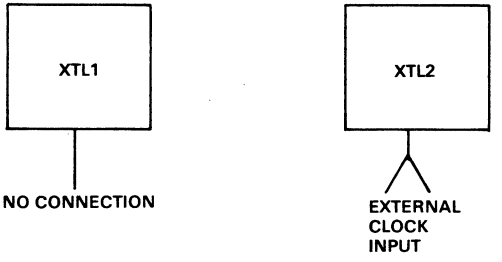
387X-10, -15
= + 16 percent

EXTERNAL CLOCK CONFIGURATION

The connection for the external clock time base configuration is shown in Figure 19. Refer to the DC Characteristics section for proper input levels and current requirements.

Refer to the Capacitance section of the appropriate 3873 Family device data sheet for input capacitance.

EXTERNAL MODE CONNECTION
Figure 19



OPERATING VOLTAGES AND TEMPERATURES

Dash Number Suffix	Operating Voltage V_{CC}	Operating Temperature T_A
—00	+5V ± 10%	0°C - 70°C
—05	+5V ± 5%	0°C - 70°C
—10	+5V ± 10%	-40°C - +85°C
—15	+5V ± 5%	-40°C - +85°C

ABSOLUTE MAXIMUM RATINGS*

	-00,-05	-10,-15
Temperature Under Bias	-20°C to +85°C	-50°C to +100°C
Storage Temperature	-65°C to +150°C	-65°C to +150°C
Voltage on any Pin With Respect to Ground (Except open drain pins and TEST)	-1.0V to +7V	-1.0V to +7V
Voltage on TEST with Respect to Ground	-1.0V to +9V	-1.0V to +9V
Voltage on Open Drain Pins With Respect to Ground	-1.0V to +13.5V	-1.0V to + 13.5V
Power Dissipation	1.5W	1.5W
Power Dissipation by any one I/O pin[2]	60mW	60mW
Power Dissipation by all I/O pins[2]	600mW	600mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC CHARACTERISTICS

T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100mW (Note 2)

SIGNAL	SYM	PARAMETER	-00,-05 MIN	-00,-05 MAX	-10,-15 MIN	-10,-15 MAX	UNIT	NOTES
XTL1 XTL2	t_0	Time Base Period, all clock modes	250	500	250	500	ns	4MHz-2MHz
	$t_{ex(H)}$	External clock pulse width high	90	400	100	390	ns	
	$t_{ex(L)}$	External clock pulse width low	100	400	110	390	ns	
Φ	t_Φ	Internal Φ clock	$2t_0$		$2t_0$			
WRITE	t_W	Internal WRITE Clock period	4tΦ 6tΦ		4tΦ 6tΦ			Short Cycle Long Cycle
I/O	$t_{dI/O}$	Output delay from internal WRITE clock	0	1000	0	1200	ns	50pF plus one TTL load
	$t_{sI/O}$	Input setup time to internal WRITE clock	1000		1200		ns	
$\overline{STROBE}$	$t_{I/O-s}$	Output valid to $\overline{STROBE}$ delay	3tΦ -1000	3tΦ +250	3tΦ -1200	3tΦ +300	ns	I/O load = 50pF + 1 TTL load
	t_{sL}	$\overline{STROBE}$ low time	8tΦ -250	12tΦ +250	8tΦ -300	12tΦ +300	ns	$\overline{STROBE}$ load = 50pF+3TTL loads
$\overline{RESET}$	t_{RH}	$\overline{RESET}$ hold time, low	6tΦ +750		6tΦ +1000		ns	
	t_{RPOC}	$\overline{RESET}$ hold time, low for power clear	power supply rise time +0.1		power supply rise time +0.15		ms	
EXT INT	t_{EH}	EXT INT hold time in active and inactive state	6tΦ +750		6tΦ +1000		ns	To trigger interrupt
			2tΦ		2tΦ		ns	To trigger timer

CAPACITANCE
T_A = 25°C
All Part Numbers

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
C_{IN}	Input capacitance; I/O, $\overline{RESET}$, EXT INT, TEST		10	pF	unmeasured pins grounded
C_{XTL}	Input capacitance; XTL1, XTL2	23.5	29.5	pF	

AC CHARACTERISTICS FOR SERIAL I/O PINS
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100mW (Note 2)

			-00, -05		-10, -15			
SIGNAL	SYM	PARAMETER	MIN	MAX	MIN	MAX	UNIT	CONDITIONS
SRCLK	$t_{C(SRCLK)}$	Serial Clock Period in External Clock Mode Async	3.25	∞	3.25	∞	μs	
		Sync	4.0	∞	4.0	∞	μs	
	$t_{W(SRCLKH)}$	Serial Clock Pulse Width, High. External Clock Mode	1.3	∞	1.3	∞	μs	
	$t_{W(SRCLKL)}$	Serial Clock Pulse Width, Low. External Clock Mode	1.3	∞	1.3	∞	μs	
	$t_{r(SRCLK)}$	Serial Clock Rise Time Internal Clock Mode		60		100	ns	0.8V –2.0V C_L = 100pf
	$t_{f(SRCLK)}$	Serial Clock Fall Time Internal Clock Mode		30		50	ns	2.4V –0.4V C_L = 100pf
SI	$t_{S(SI)}$	Setup Time To Rising Edge of SRCLK (SYNC Mode)	0		0		ns	
	$t_{H(SI)}$	Hold Time From Rising Edge of SRCLK (SYNC Mode)	2		2		μs	
SO	$t_{D(SO)}$	Data Output Delay From Falling Edge of SRCLK (SYNC Mode)		1190		1190	ns	

AC CHARACTERISTICS FOR MK38P73

(Signals brought out at socket)
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100mW (Note 2)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	CONDITION
		MIN	MAX	MIN	MAX		
t_{aas}*	Access time from Address A_{11}-A_{01} stable until data must be valid at D_7-D_0	650		650		ns	Φ = 2.0MHz

*See Table in Figure 13.

DC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100mW (Note 2)

SYM	PARAMETER	-00,-05		-10,-15		UNIT	DEVICE
		MIN	MAX	MIN	MAX		
I_{CC}	Average Power Supply Current		93.5		121	mA	MK3873/10 Outputs Open
			103		138	mA	MK3873/12 Outputs Open
			93.5		121	mA	MK3873/20 Outputs Open
			103		138	mA	MK3873/22 Outputs Open
			138		165	mA	MK38P73/02 No EPROM, Outputs Open
P_D	Power Dissipation		440		570	mW	MK3873/10 Outputs Open
			485		645	mW	MK3873/12 Outputs Open
			440		570	mW	MK3873/20 Outputs Open
			485		645	mW	MK3873/22 Outputs Open
			646		775	mW	MK38P73/02 No EPROM, Outputs Open

DC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100mW (Note 2)

SYM	PARAMETER	-00,-05		-10,-15		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{IHEX}	External Clock input high level	2.4	5.8	2.4	5.8	V	
V_{ILEX}	External Clock input low level	-.3	.6	-.3	.6	V	
I_{IHEX}	External Clock input high current		100		130	μA	$V_{IHEX}=V_{CC}$
I_{ILEX}	External Clock input low current		-100		-130	μA	$V_{ILEX}=V_{SS}$
$V_{IHI/O}$	I/O input high level	2.0	5.8	2.0	5.8	V	standard pull-up (1)
		2.0	13.2	2.0	13.2	V	open drain (1)
V_{IHR}	Input high level, $\overline{RESET}$	2.0	5.8	2.2	5.8	V	standard pull-up (1)
		2.0	13.2	2.2	13.2	V	No pull-up
V_{IHEI}	Input high level, EXT INT	2.0	5.8	2.2	5.8	V	standard pull-up (1)
		2.0	13.2	2.2	13.2	V	No pull-up
V_{IL}	I/O ports, $\overline{RESET}$[1], EXT INT[1] input low level	-.3	.8	-.3	0.7	V	(1)
I_{IL}	Input low current, standard pull-up pins		-1.6		-1.9	mA	$V_{IN}=0.4V$
I_L	Input leakage current, open drain pins $\overline{RESET}$ and EXT INT inputs With no pull-up resistor		+10 -5		+18 -8	μA μA	$V_{IN}=13.2V$ $V_{IN}=0.0V$
I_{OH}	Output high current, standard	-100		-89		μA	$V_{OH}=2.4V$
	pull-up pins	-30		-25		μA	$V_{OH}=3.9V$
I_{OHDD}	Output high current,	-100		-80		μA	$V_{OH}=2.4V$
	direct drive pins	-1.5	-8.5	-1.3	-11	mA mA	$V_{OH}=1.5V$ $V_{OH}=0.7V$
I_{OL}	Output low current, I/O ports	1.8		1.65		mA	$V_{OL}=0.4V$
I_{OHS}	$\overline{STROBE}$ Output High current	-300		-270		μA	$V_{OH}=2.4V$
I_{OLS}	$\overline{STROBE}$ output low current	5.0		4.5		mA	$V_{OL}=0.4V$

VIII

DC CHARACTERISTICS FOR MK38P73

(Signals brought out at socket)

T_A, V_{CC} within specifiec operating range, I/O Power Dissipation ≤ 100mW. (Note 2)

SYM	PARAMETER	-00, -05		-10, -15		UNIT	CONDITION
		MIN	MAX	MIN	MAX		
	Power Supply Current for EPROM		-185		-185	mA	
V_{IL}	Input Low Level Data bus in	-0.3	0.8	-0.3	0.7	V	
V_{IH}	Input High Level Data bus in	2.0	5.8	2.0	5.8	V	
I_{OH}	Output High Current	-100 -30		-90 -25		μA μA	V_{OH}=2.4V V_{OH}=3.9V
I_{OL}	Output Low Current	1.8		1.65		mA	V_{OL}=0.4V
I_{IL}	Input Leakage Current		10		10	μA	Data Bus in Float

DC CHARACTERISTICS FOR SERIAL PORT I/O PINS

T_A, V_{CC} within specified operating range

I/O Power Dissipation ≤ 100mW (Note 2)

SYM	PARAMETER	-00, -05		-10, -15		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
V_{IHS}	Input High for SI, SRCLK	2.0	5.8	2.0	5.8	V	
V_{ILS}	Input Low level for SI, SRCLK	-.3	.8	-.3	0.7	V	
I_{ILS}	Input low current for SI, SRCLK		-1.6		-1.9	mA	V_{IL} = 0.4V
I_{OHSO}	Output High Current SO	-100 -30		-90 -25		μA μA	V_{OH} = 2.4V V_{OL} = 3.9V
I_{OLSO}	Output Low Current SO	1.8		1.65		mA	V_{OL} = 0.4V
I_{OHSRC}	Output High Current SRCLK	-300		-270		μA	V_{OH} = 2.4V
I_{OLSRC}	Output Low Current SRCLK	5.0		4.5		mA	V_{OL} = 0.4V

1. $\overline{\text{RESET}}$ and EXT INT have internal Schmit triggers giving minimum .2V hysteresis.
2. Power dissipation for I/O pins is calculated by $\Sigma (V_{CC} - V_{IL})(I_{IL}) + \Sigma (V_{CC} - V_{OH})(I_{OH}) + \Sigma (V_{OL})(I_{OL})$

TIMER AC CHARACTERISTICS

Definitions:

Error = Indicated time value - actual time value

tpsc = t Φ x Prescale Value

Interval Timer Mode:

Single interval error, free running (Note 3) ..... ±6tΦ
Cumulative interval error, free running (Note 3) 0
Error between two Timer reads (Note 2) ..... ± (tpsc + tΦ
Start Timer to stop Timer error (Notes 1,4) ..... +tΦ to —(tpsc +tΦ)
Start Timer to read Timer error (Notes 1,2) ..... —5tΦ to —(tpsc + 7tΦ)
Start Timer to interrupt request error (Notes 1,3) ..... —2tΦ to —8tΦ)
Load Timer to stop Timer error (Note 1) ..... +tΦ to —(tpsc + 2tΦ)
Load Timer to read Timer error (Notes 1,2) ..... —5tΦ to —(tpsc + 8tΦ)
Load Timer to interrupt request error (Notes 1,3) ..... —2tΦ to —9tΦ)

Pulse Width Measurement Mode:

Measurement accuracy (Note 4)	+t Φ to —(tpsc +2t Φ)
Minimum pulse width of EXT INT pin	2tΦ

Event Counter Mode:

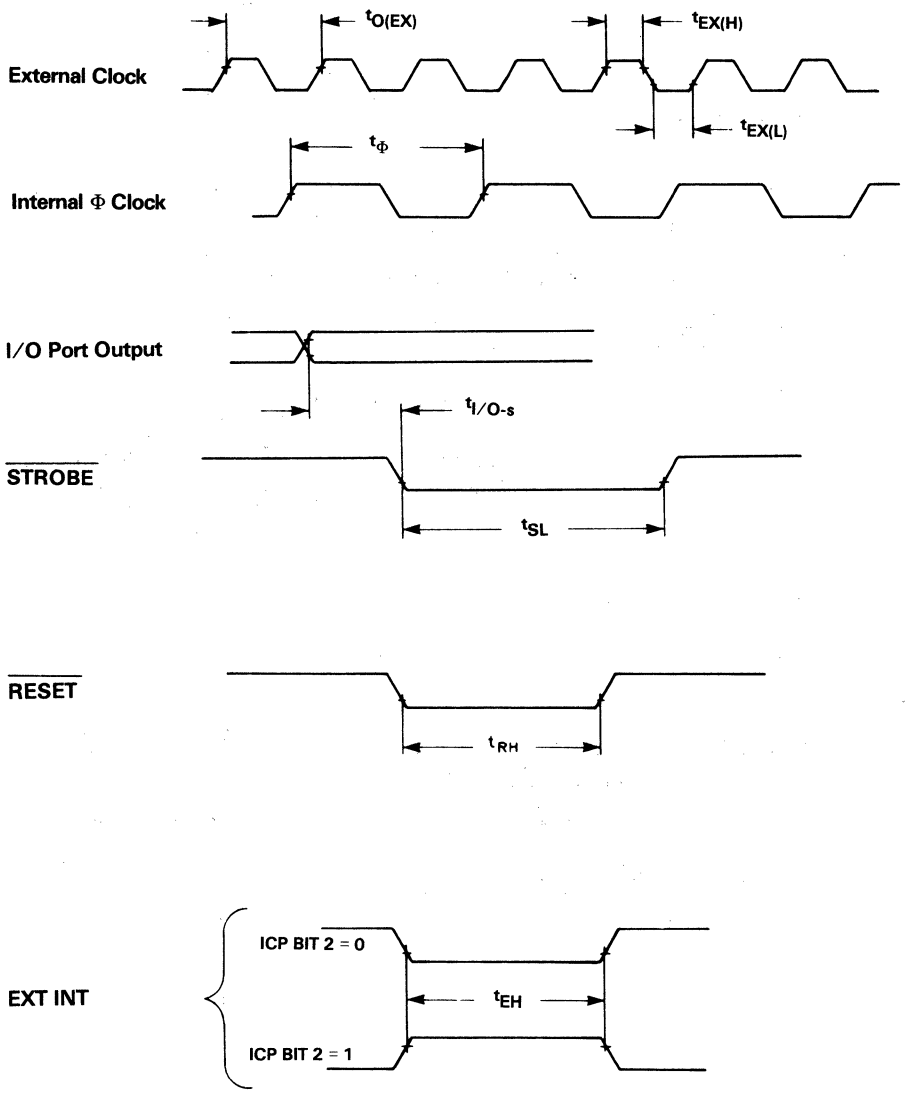
Minimum active time of EXT INT pin	2tΦ
Minimum inactive time of EXT INT pin	2tΦ

Notes:

1. All times which entail loading, starting, or stopping the Timer are referenced from the end of the last machine cycle of the OUT or OUTS instruction.
2. All times which entail reading the Timer are referenced from the end of the last machine cycle of the IN or INS instruction.
3. All times which entail the generation of an interrupt request are referenced from the start of the machine cycle in which the appropriate interrupt request latch is set. Additional time may elapse if the interrupt request occurs during a privileged or multicycle instruction.
4. Error may be cumulative if operation is repetitively performed.

AC TIMING DIAGRAM

Figure 20

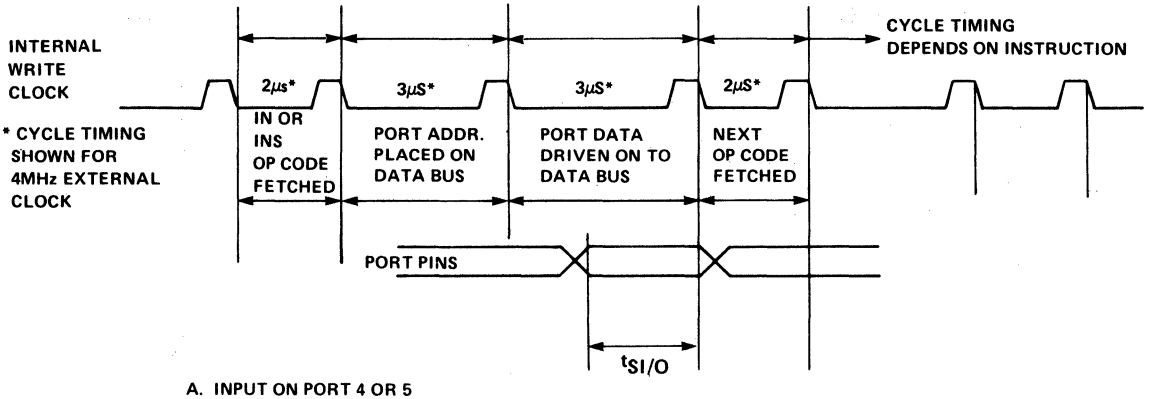


Note: All AC measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} (.8v), or V_{OH} (2.0v).

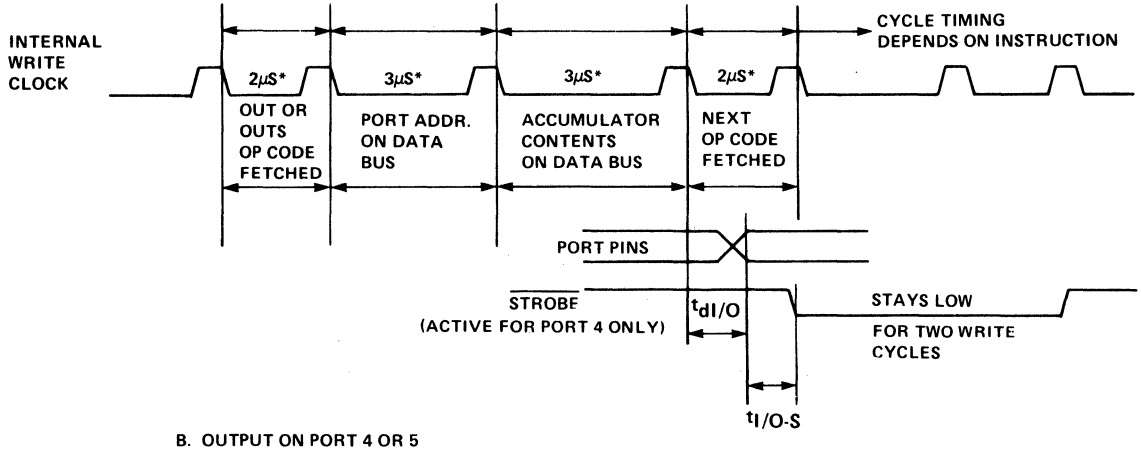
VIII

INPUT/OUTPUT AC TIMING

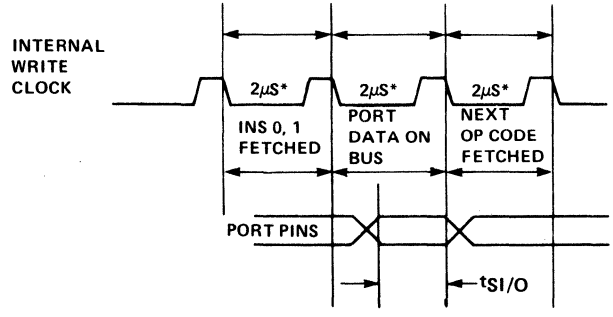
Figure 21



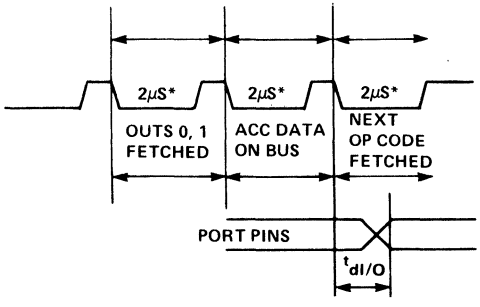
A. INPUT ON PORT 4 OR 5



B. OUTPUT ON PORT 4 OR 5



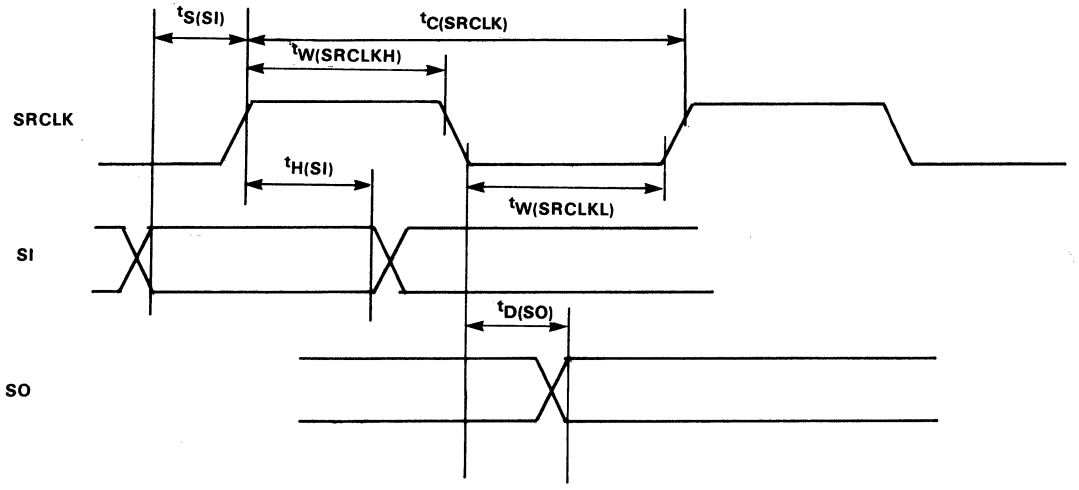
C. INPUT ON PORT 0 OR 1



D. OUTPUT ON PORT 0, 1

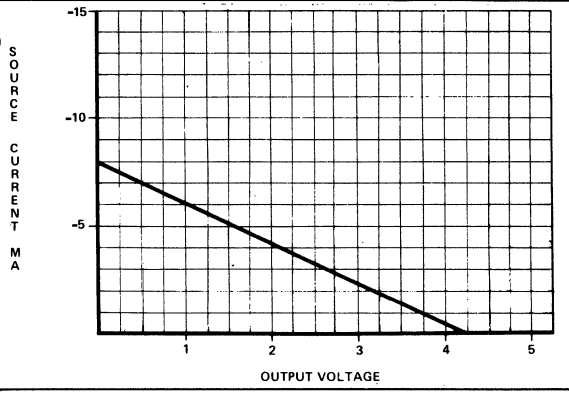
AC TIMING DIAGRAM FOR SERIAL I/O PINS.

Figure 22



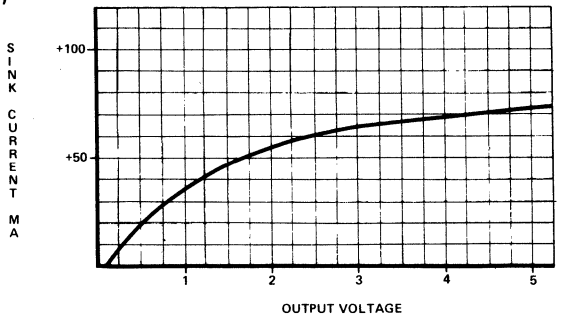
STROBE SOURCE CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

Figure 23



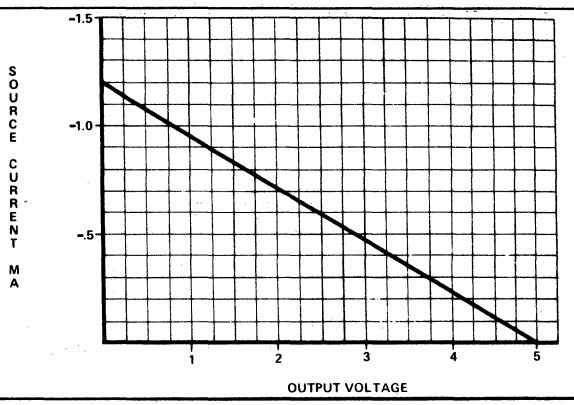
STROBE SINK CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

Figure 24

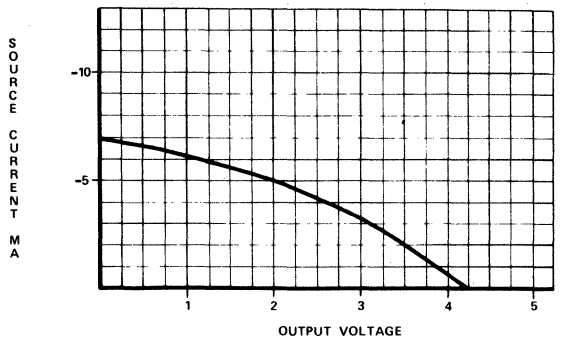


VIII

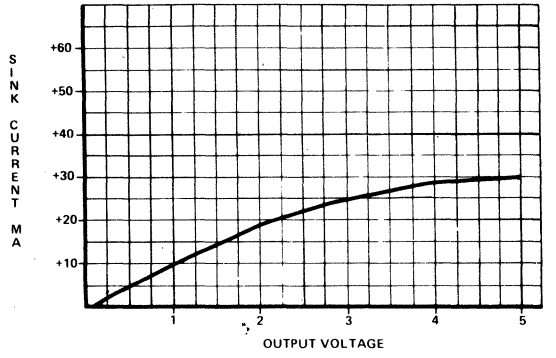
STANDARD I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 25



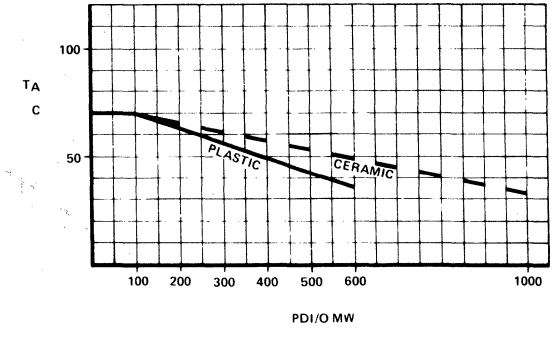
DIRECT DRIVE I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 26



I/O PORT SINK CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 27



MAXIMUM OPERATING TEMPERATURE VS. I/O POWER DISSIPATION
Figure 28

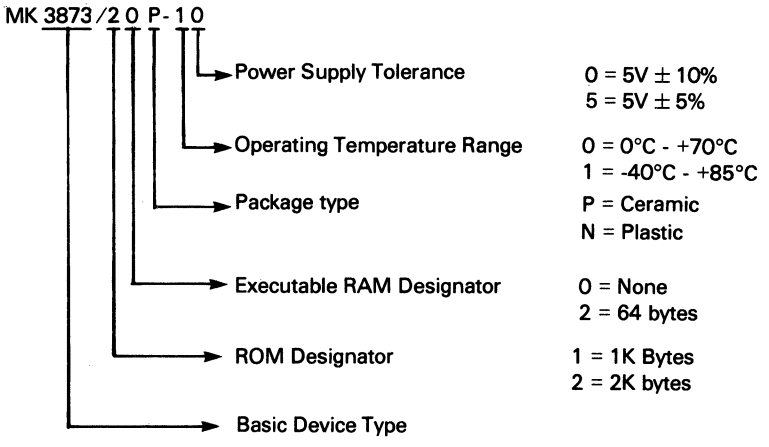


ORDERING INFORMATION

There are two types of part numbers for the 3870 family of devices. The generic part number describes the basic device type, the amount of ROM and Executable RAM, the desired package type, temperature range, and power supply tolerance. For each customer specific code, additional information defining I/O options and oscillator options will be combined with the information described in the generic part number to define a customer/code specific device order number.

GENERIC PART NUMBER

An example of the generic part number is shown below.

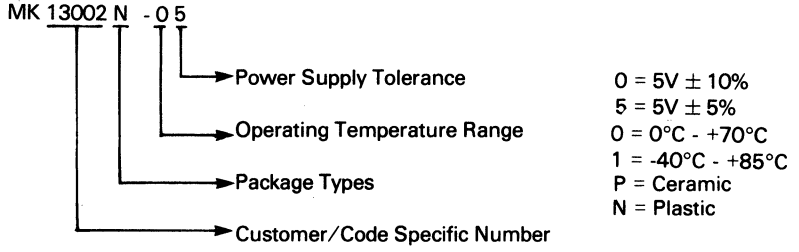


An example of the generic part number for the PPROM device is shown below.

MK38P73/02 R-05

DEVICE ORDER NUMBER

An example of the device order number is shown below.



The Customer/Code specific number defines the ROM bit pattern, I/O configuration, oscillator type, and generic part type to be used to satisfy the requirements of a particular customer purchase order. For further information on the ordering of mask ROM devices, the customer should refer to the 3870 Family Technical Manual.